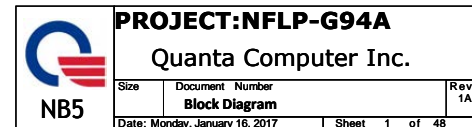
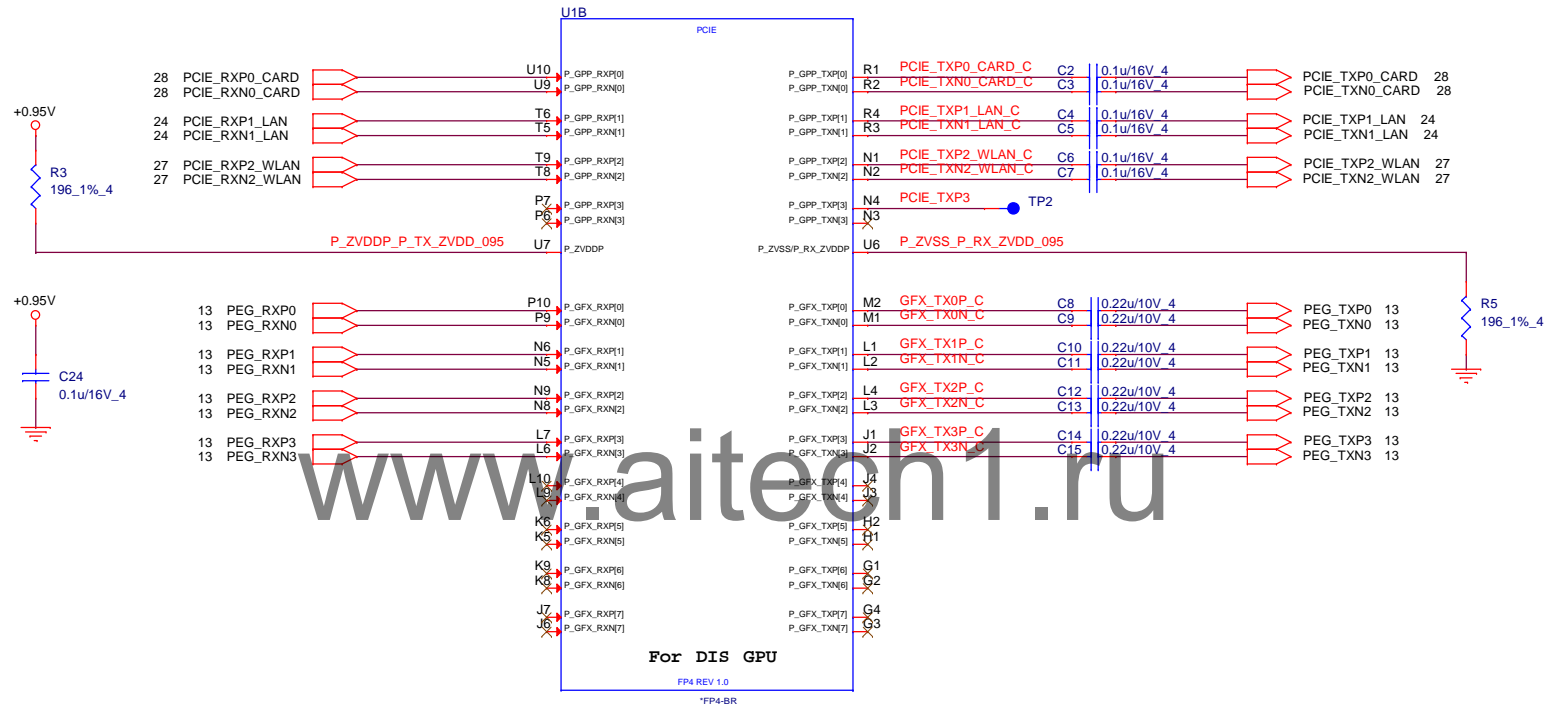


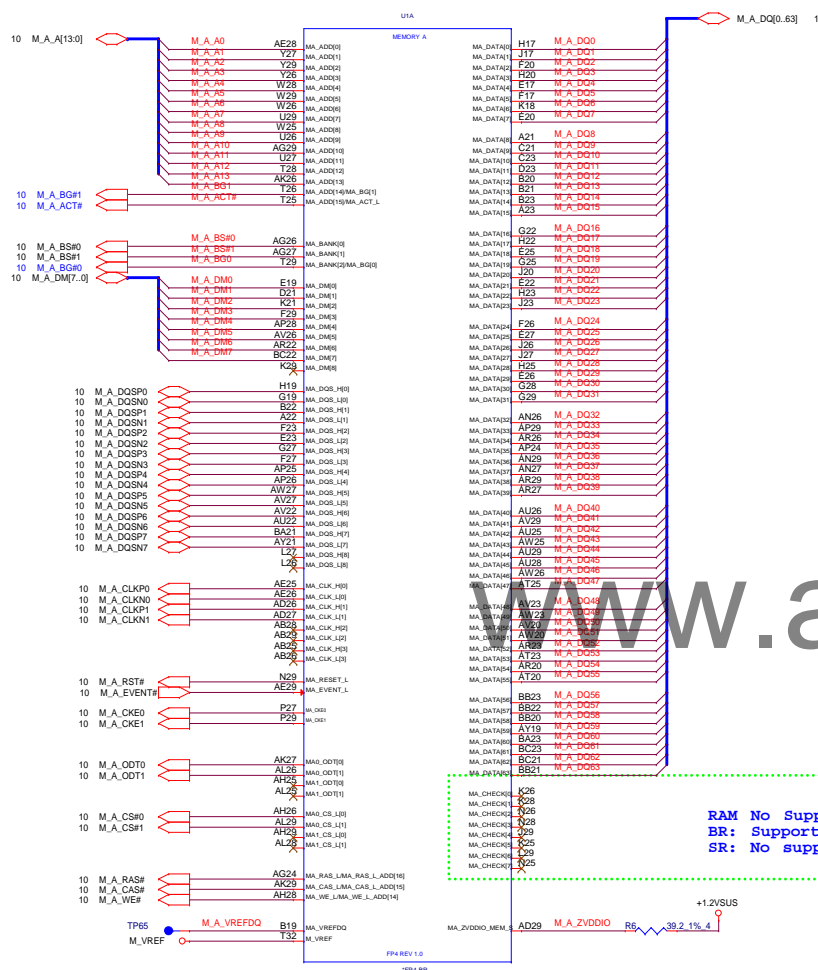
## PCB 8L STACK UP



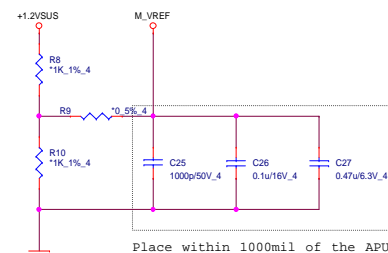


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	BR & SR 1/7(PCIE)		1A
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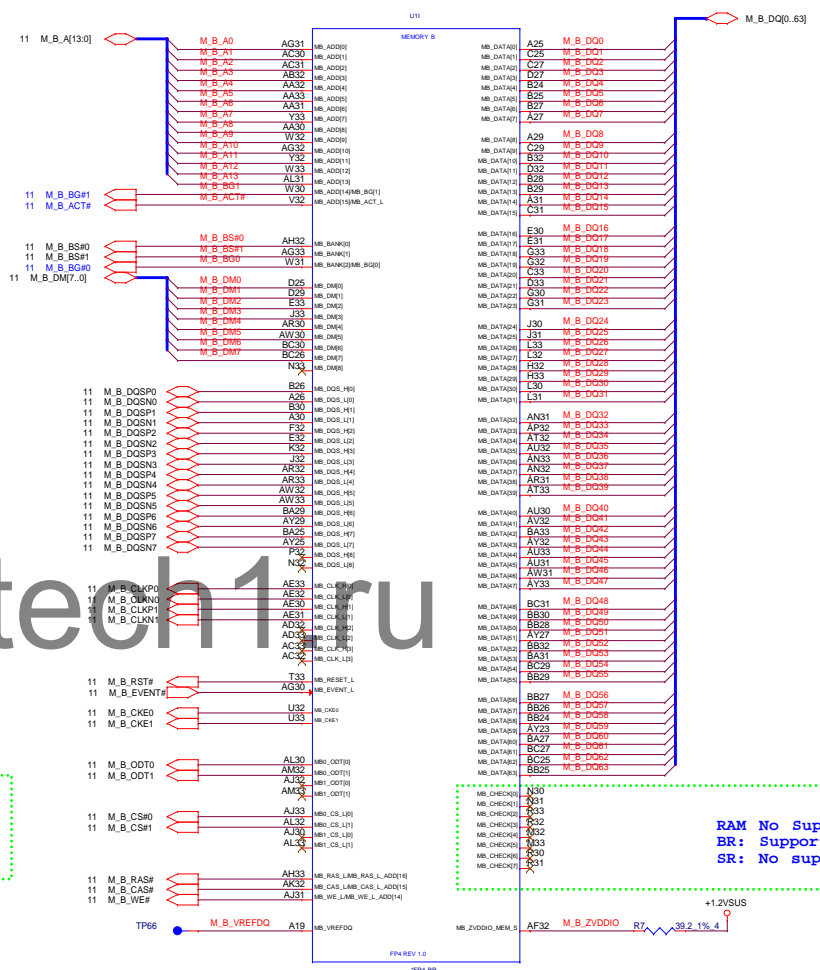
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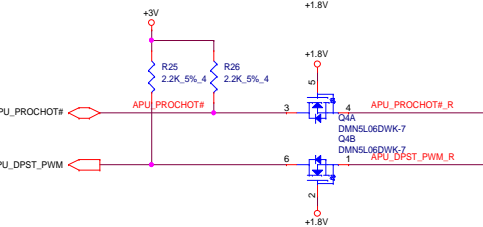
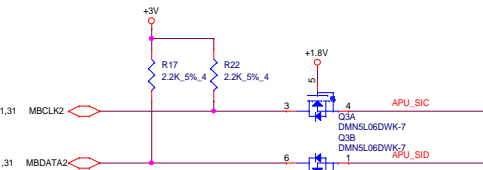
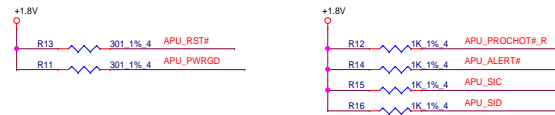
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BR: Support ECC
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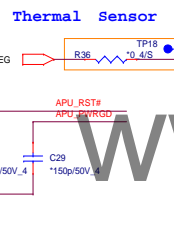
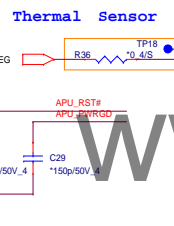
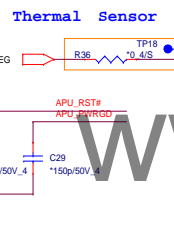
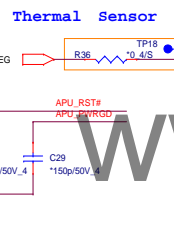
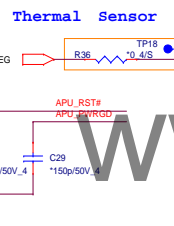
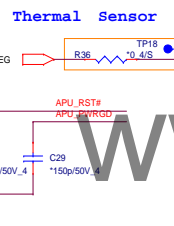
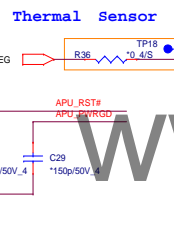
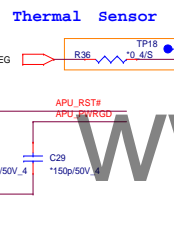
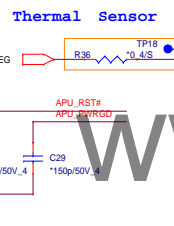
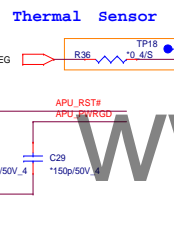
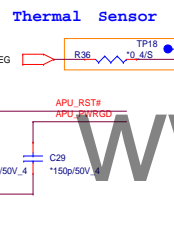
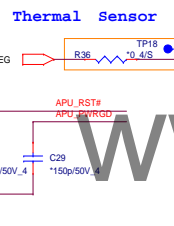
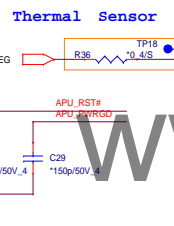
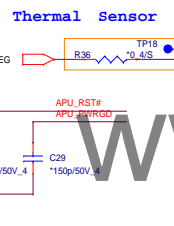
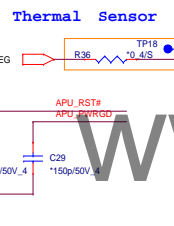
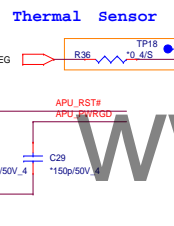
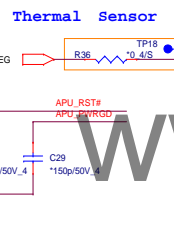
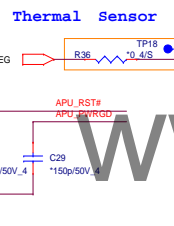
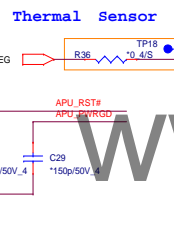
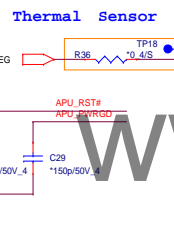
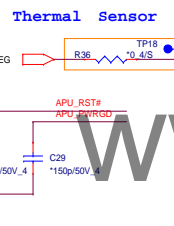
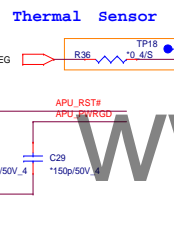
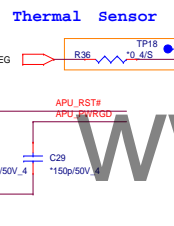
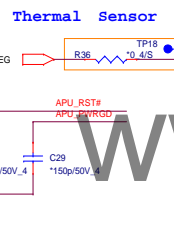
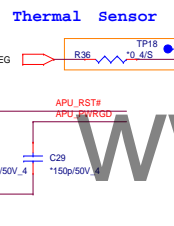
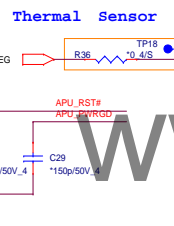
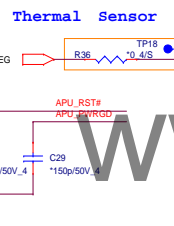
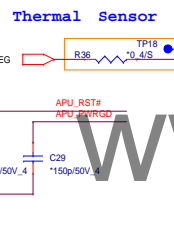
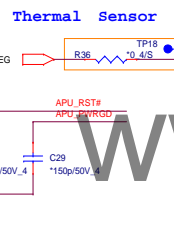
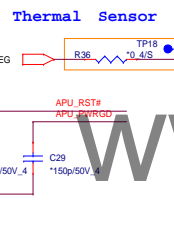
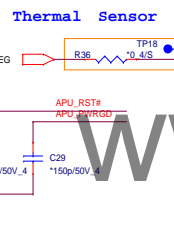
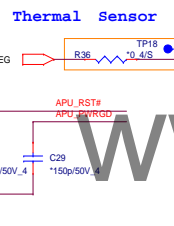
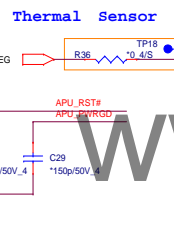
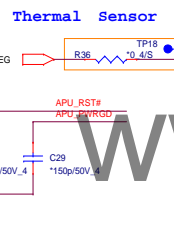
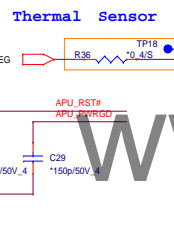
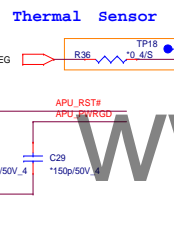
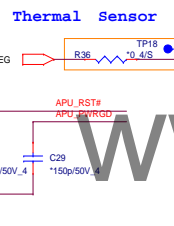
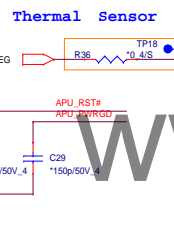
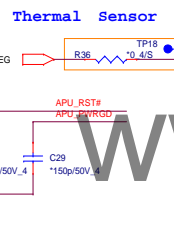
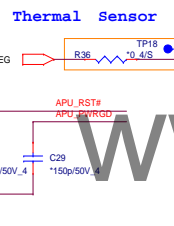
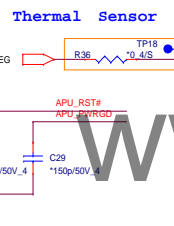
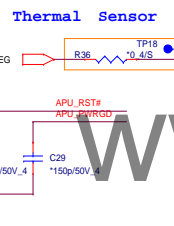
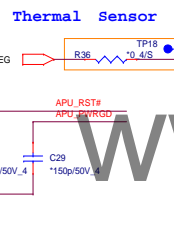
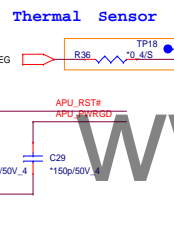
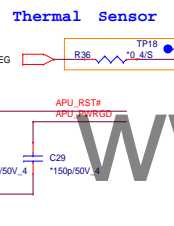
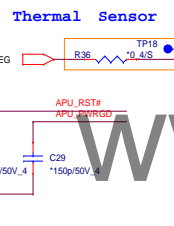
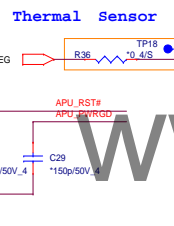
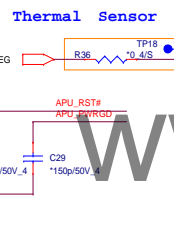
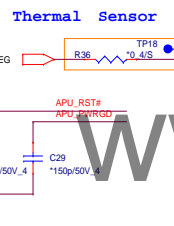
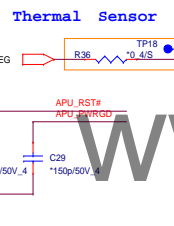
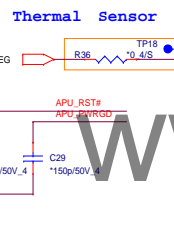
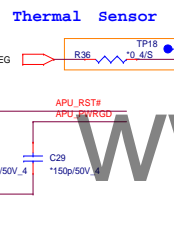
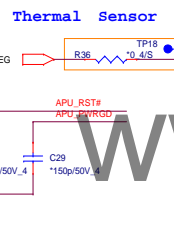
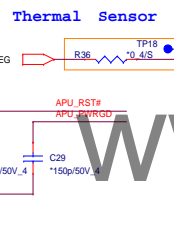
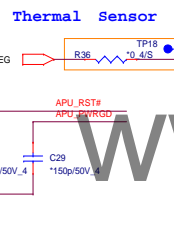
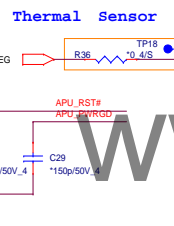
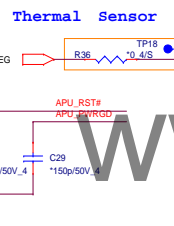
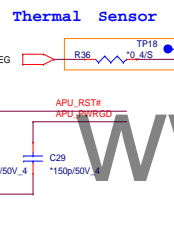
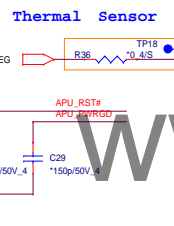
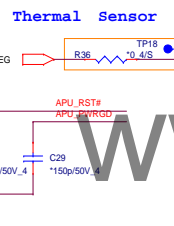
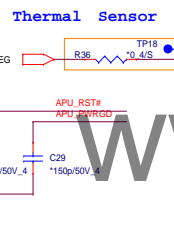
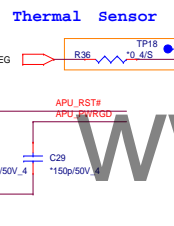
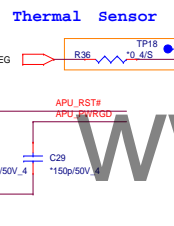
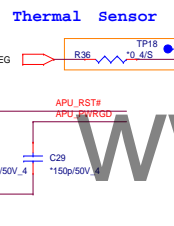
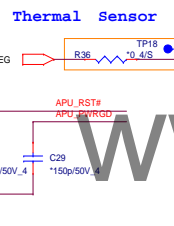
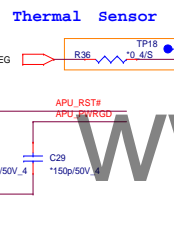
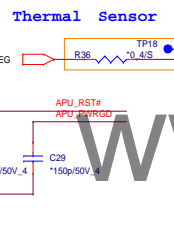
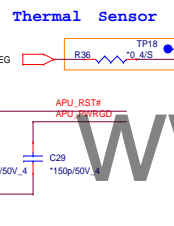
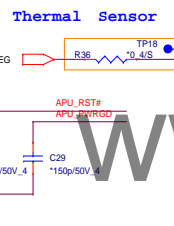
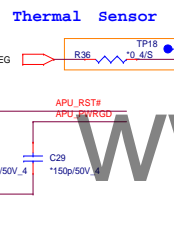
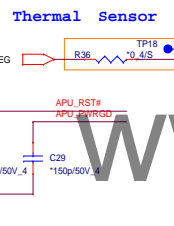
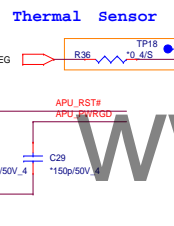
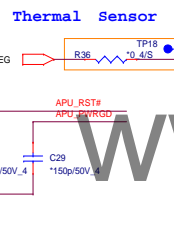
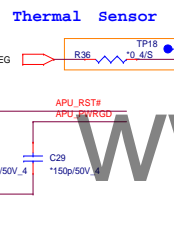
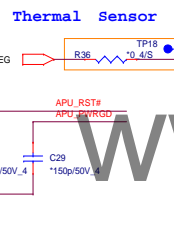
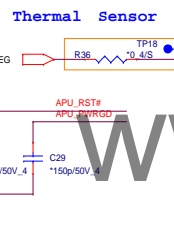
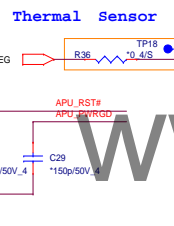
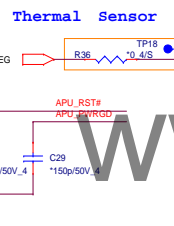
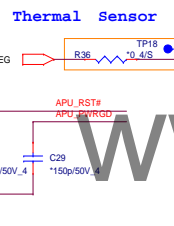
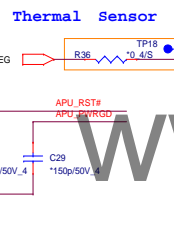
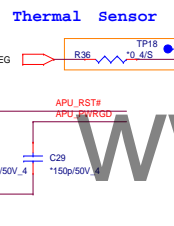
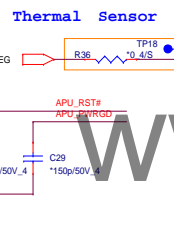
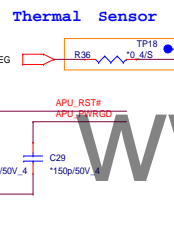
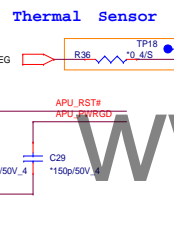
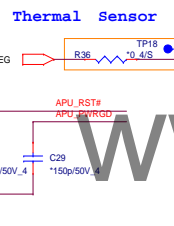
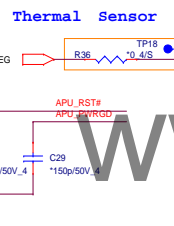
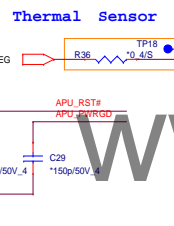
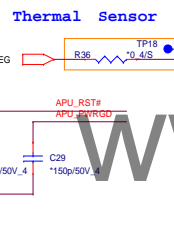
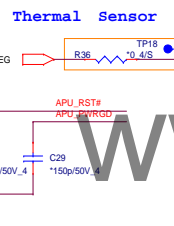
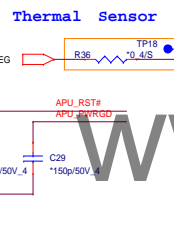
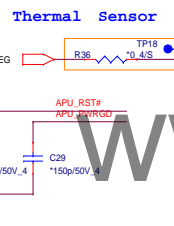
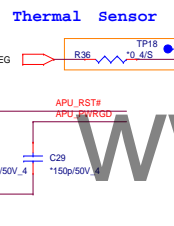
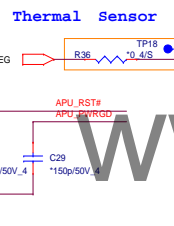
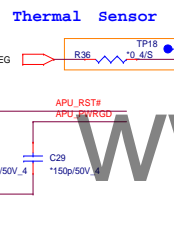
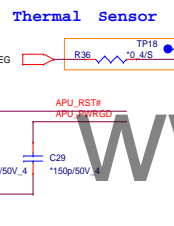
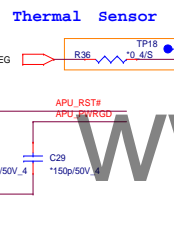
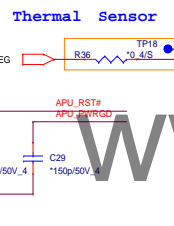
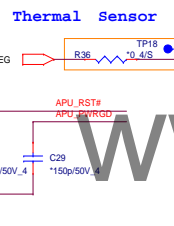
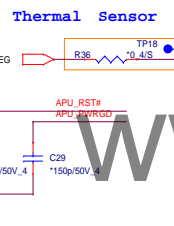
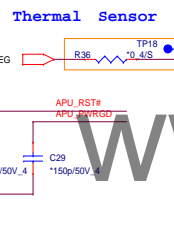
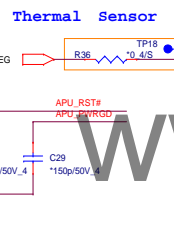
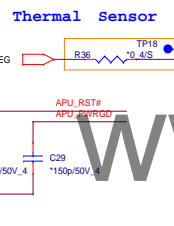
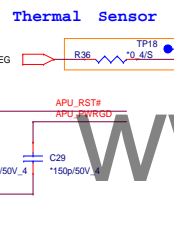
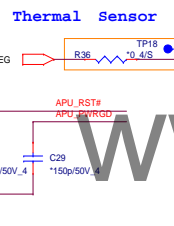
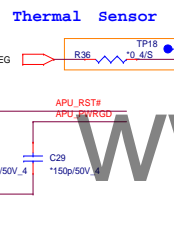
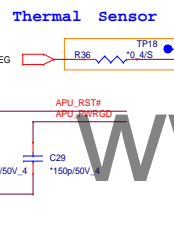
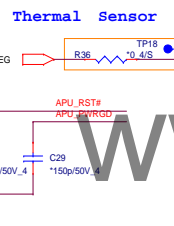
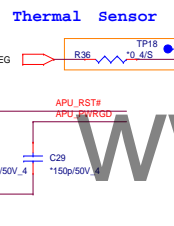
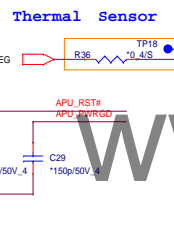
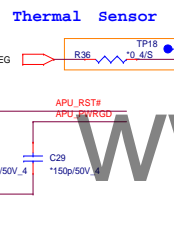
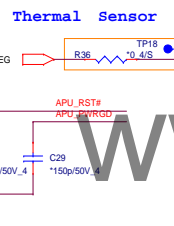
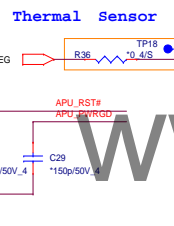
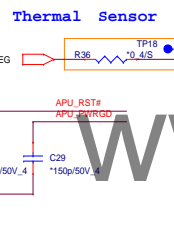
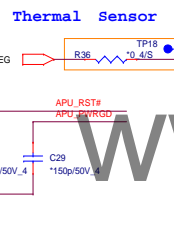
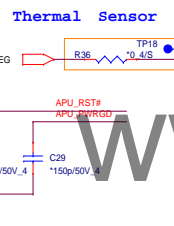
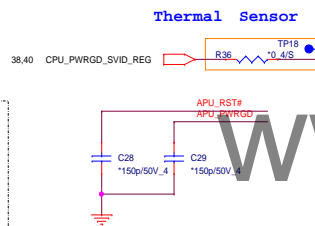
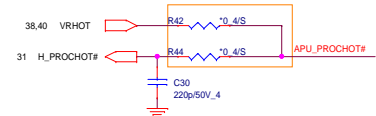
Place within 1000mil of the APU



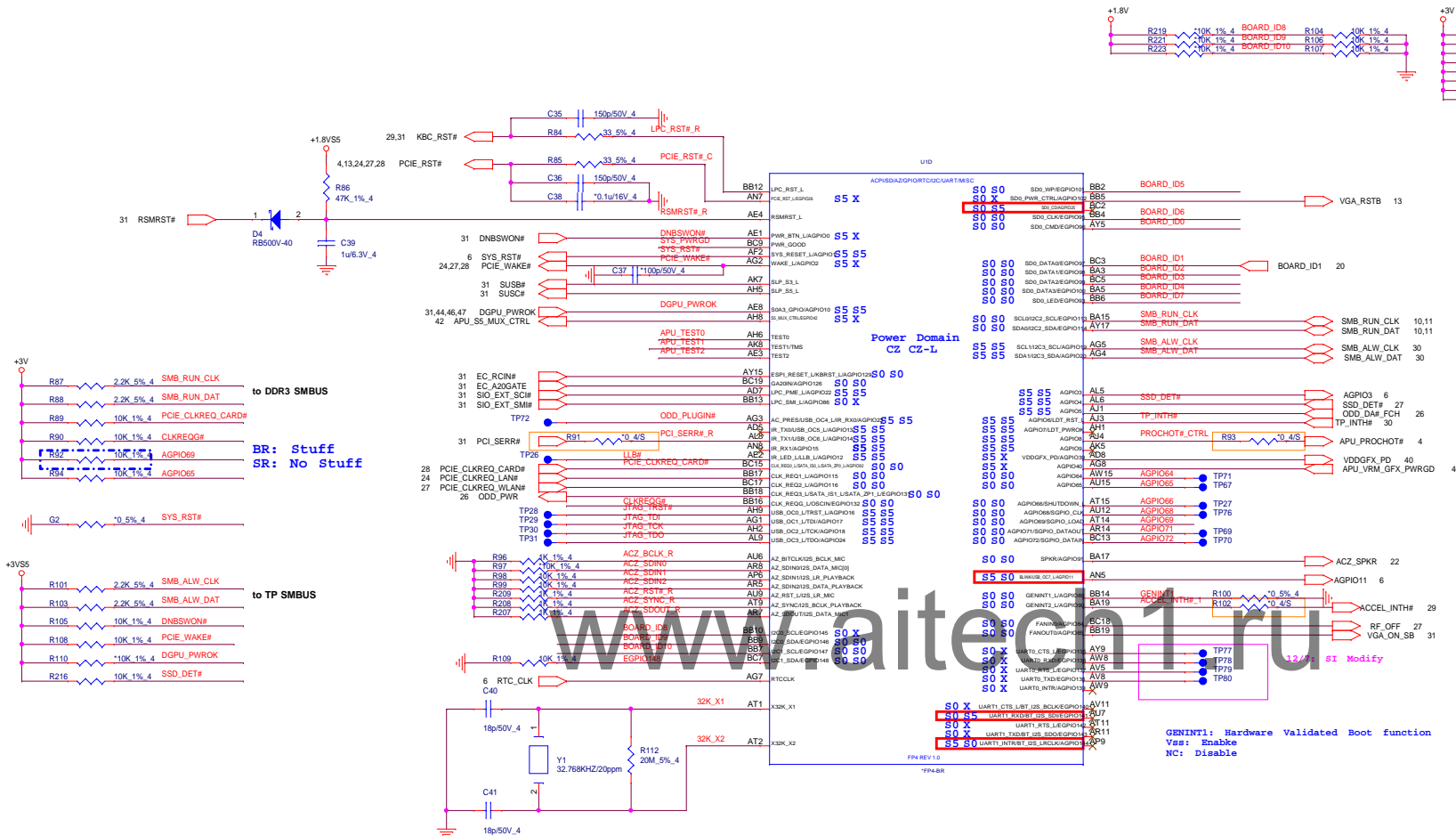
```
RAM No Support
BR: Support ECC
SR: No support ECC
```



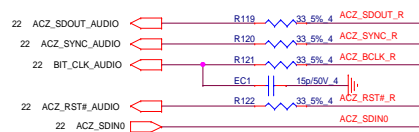
### EC H\_PROCHOT#



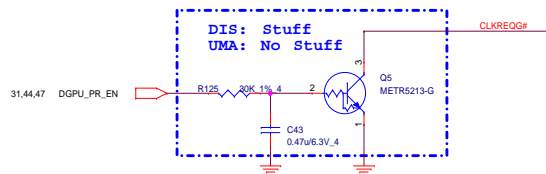




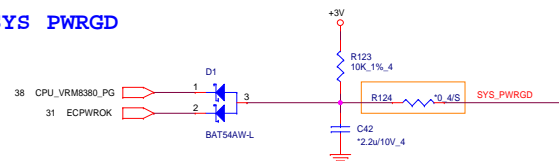
## HDA INTERFACE



## GPU CLK REQ



## SYS PWRGD



Follow AMD checklist 53537\_1.09 suggestion.

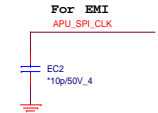
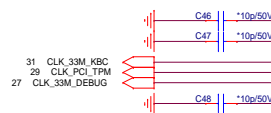
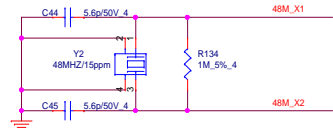
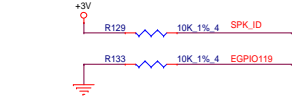


TEST2	TEST1	TEST0	Description
0	0	0	FCH JTAG accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



## Follow Checklist

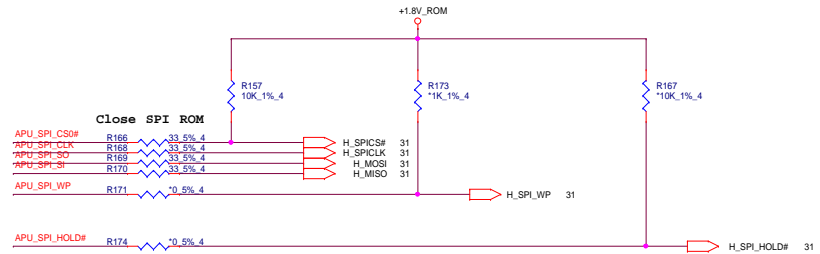
OPTION: ODD or SSD(M.2)



For EMI  
APU\_SPI\_CLK

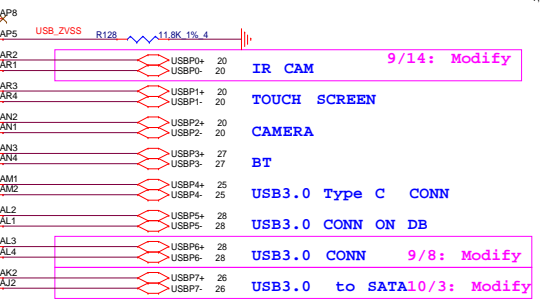
## APU SPI ROM

Vender	Size	P/N (1.8V)
WND	8M	AKE5EZN0N00
EON	8M	AKE5EFN0Q00
	8M	
Socket	DFHS08FS023	



## U1E

CLKSATAUSBSPICFC  
USBCLOCK20M,48M,OSC



IR CAM 9/14: Modify

TOUCH SCREEN

CAMERA

BT

USB3.0 Type C CONN

USB3.0 CONN ON DB

USB3.0 CONN 9/8: Modify

USB3.0 to SATA10/3: Modify

USB2 &amp; USB3 MAPPING (Use form Port4)

USB2 PORT4 =&gt; USB3 PORT0

USB2 PORT5 =&gt; USB3 PORT1

USB2 PORT6 =&gt; USB3 PORT2

USB2 PORT7 =&gt; USB3 PORT3

Support S3-S5 wake up

USB3.0 C CONN ON MB

USB3.0 CONN ON DB

USB3.0 CONN ON MB

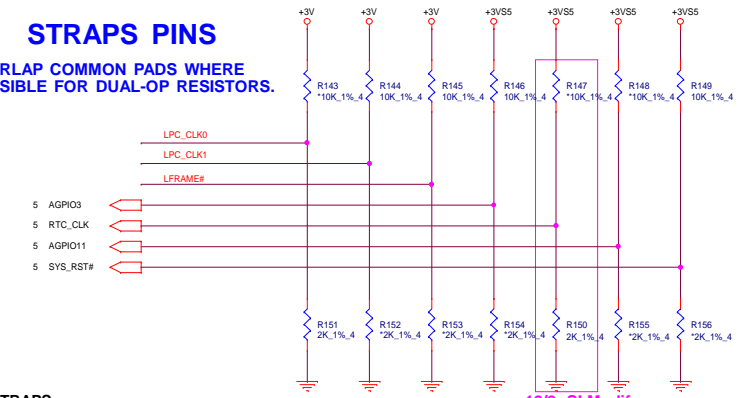
USB3.0 TO Sata ODD

9/8: New add



## STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



## REQUIRED STRAPS

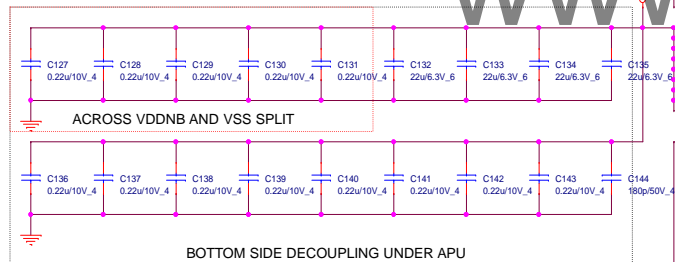
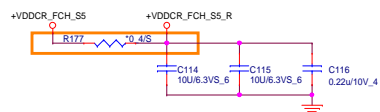
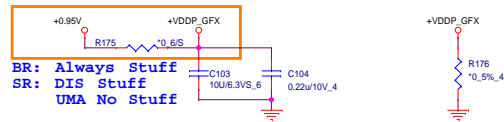
	LPC_CLK0	LPC_CLK1	LFRAME#	AGPIO3 Int Pull-Up	RTC_CLK Int Pull-Up	AGPIO11=BLINK Int Pull-Up	SYS_RST# Int Pull-Up
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM Enhanced reset logic (for quicker S5 resume) DEFAULT	Coin battery is on board. DEFAULT	LDT_RST#LDT_PWRGD output to APU DEFAULT	normal reset mode DEFAULT
PULL LOW	BOOT FAIL TIMER DISABLED	Use 100Mhz PCIE clock as reference clock and generate internal clocks only DEFAULT	LPC ROM DEFAULT	3.3V SPI ROM Default to traditional reset logic DEFAULT	Coin battery is not on board. DEFAULT	LDT_RST#LDT_PWRGD output to Pads DEFAULT	short reset mode DEFAULT



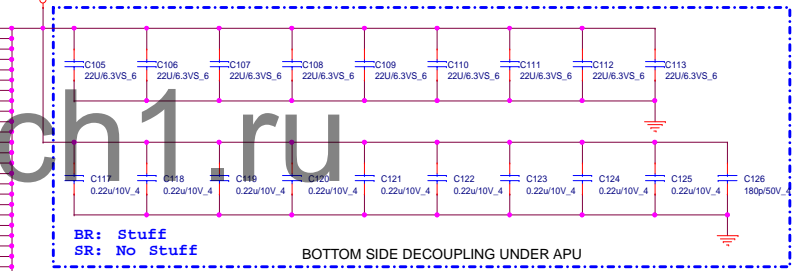
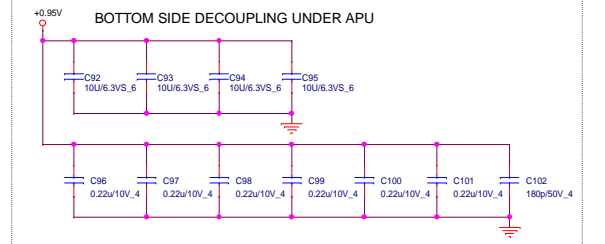
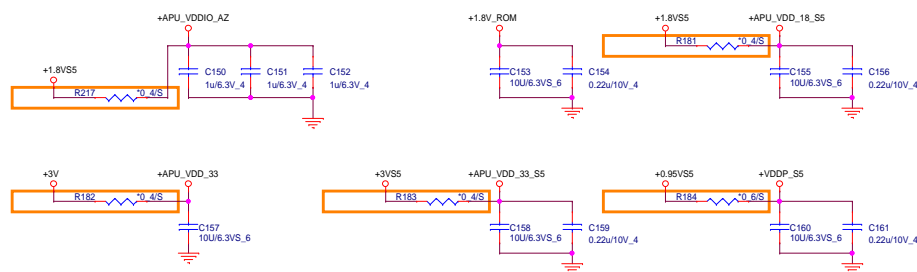
## PROJECT:NFLP-G94A

Quanta Computer Inc.

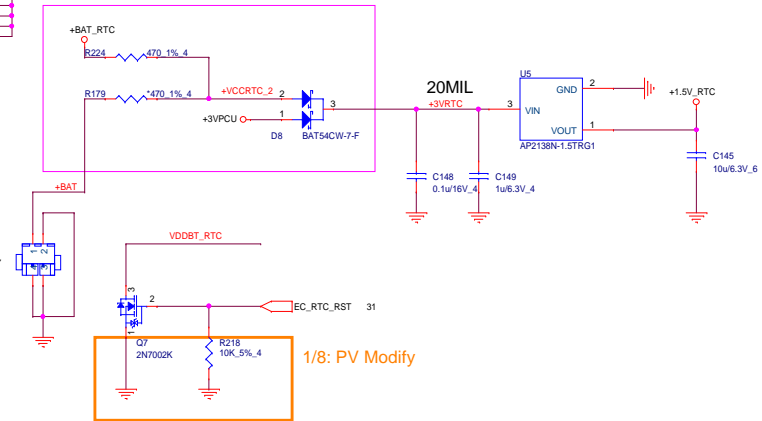
Size	Document Number	Rev
	BR & SR 5/7(SATA/USB/SPI)	1A
Date: Monday, January 16, 2017	Sheet	6 of 48

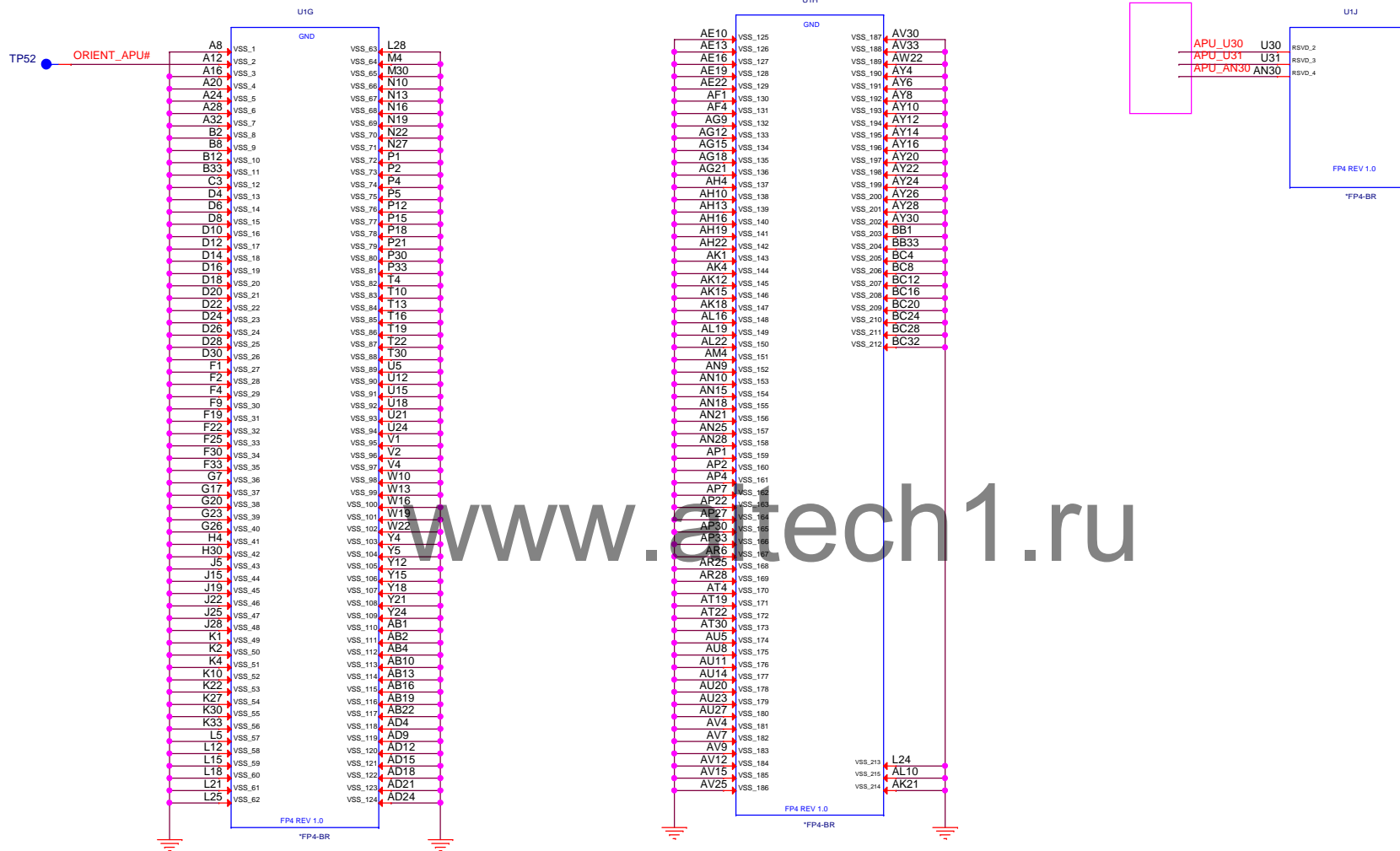


1.5V For HDA Only  
1.8V For HDA or I2S



12/2: SI Modify



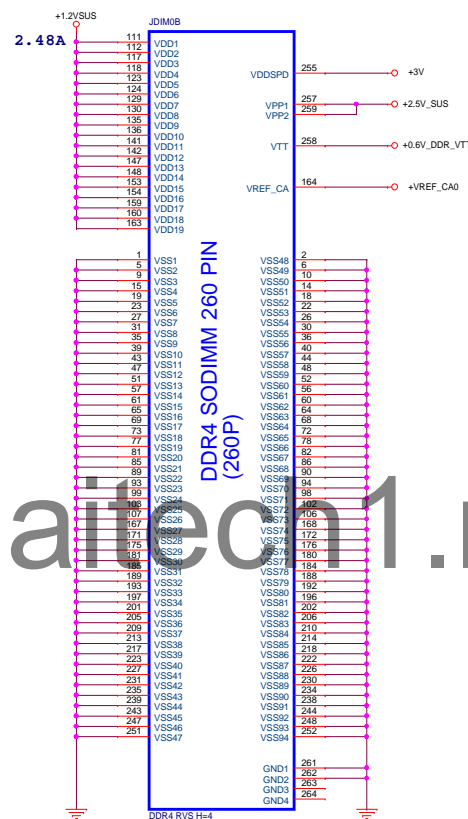
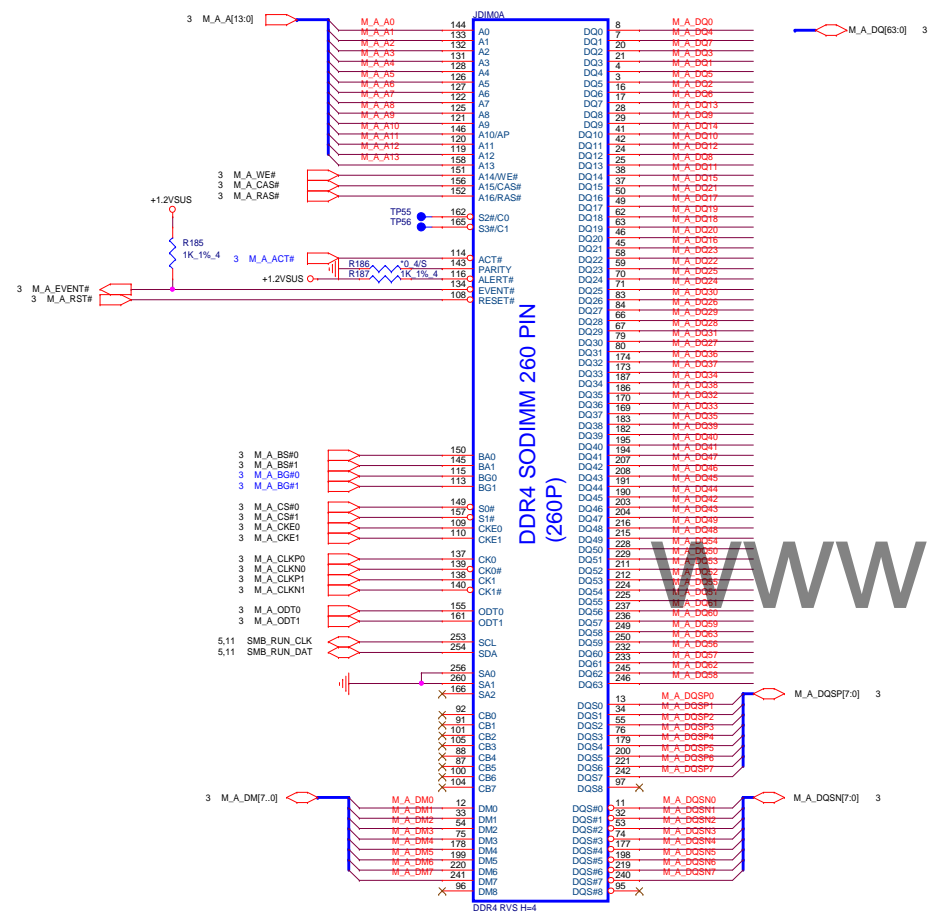
**PROJECT:NFLP-G94A**

Quanta Computer Inc.

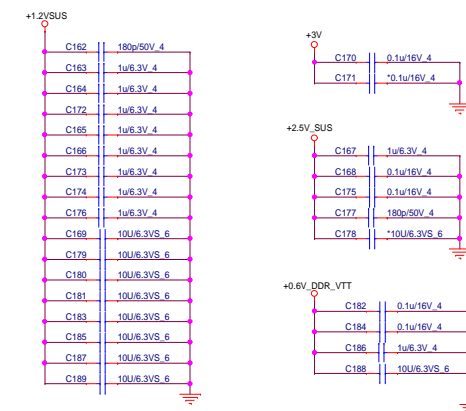
Size	Document Number	Rev
	BR & SR 7/7 (GND)	1A
Date: Monday, January 16, 2017		Sheet 8 of 48

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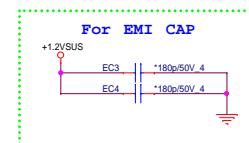
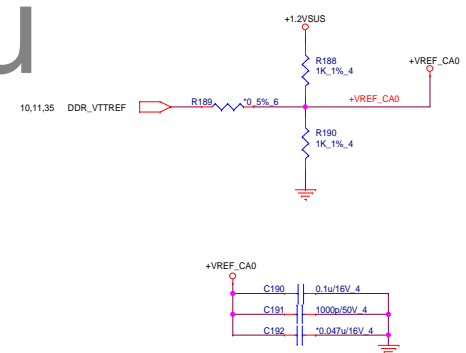
www.aitech1.ru



Place these Caps near SODIMM



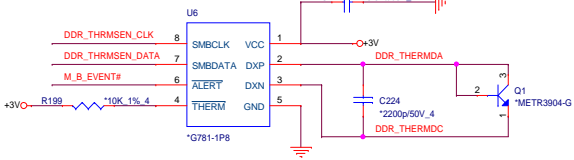
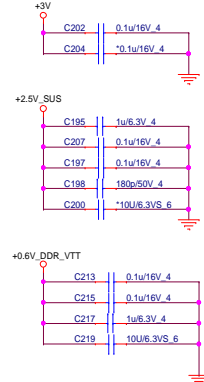
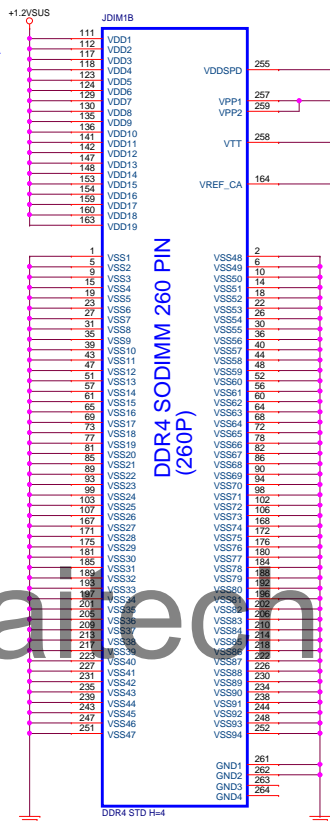
1uF/10uF 4pcs on each side of SODIMM



PROJECT: NFLP-G94A

Quanta Computer Inc.


Size C Document Number  
CHA DDR4 DIMM0-RV5(4.0H)  
Date: Monday, January 16, 2017 Sheet 10 of 48



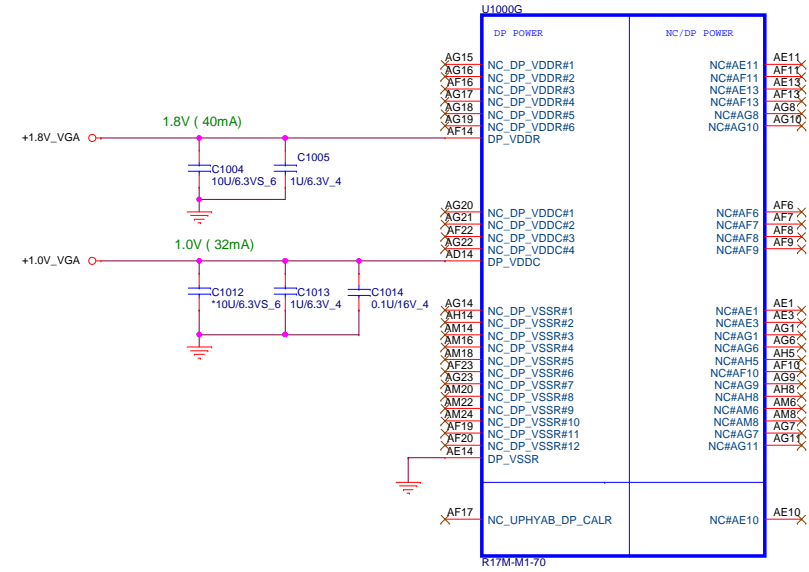
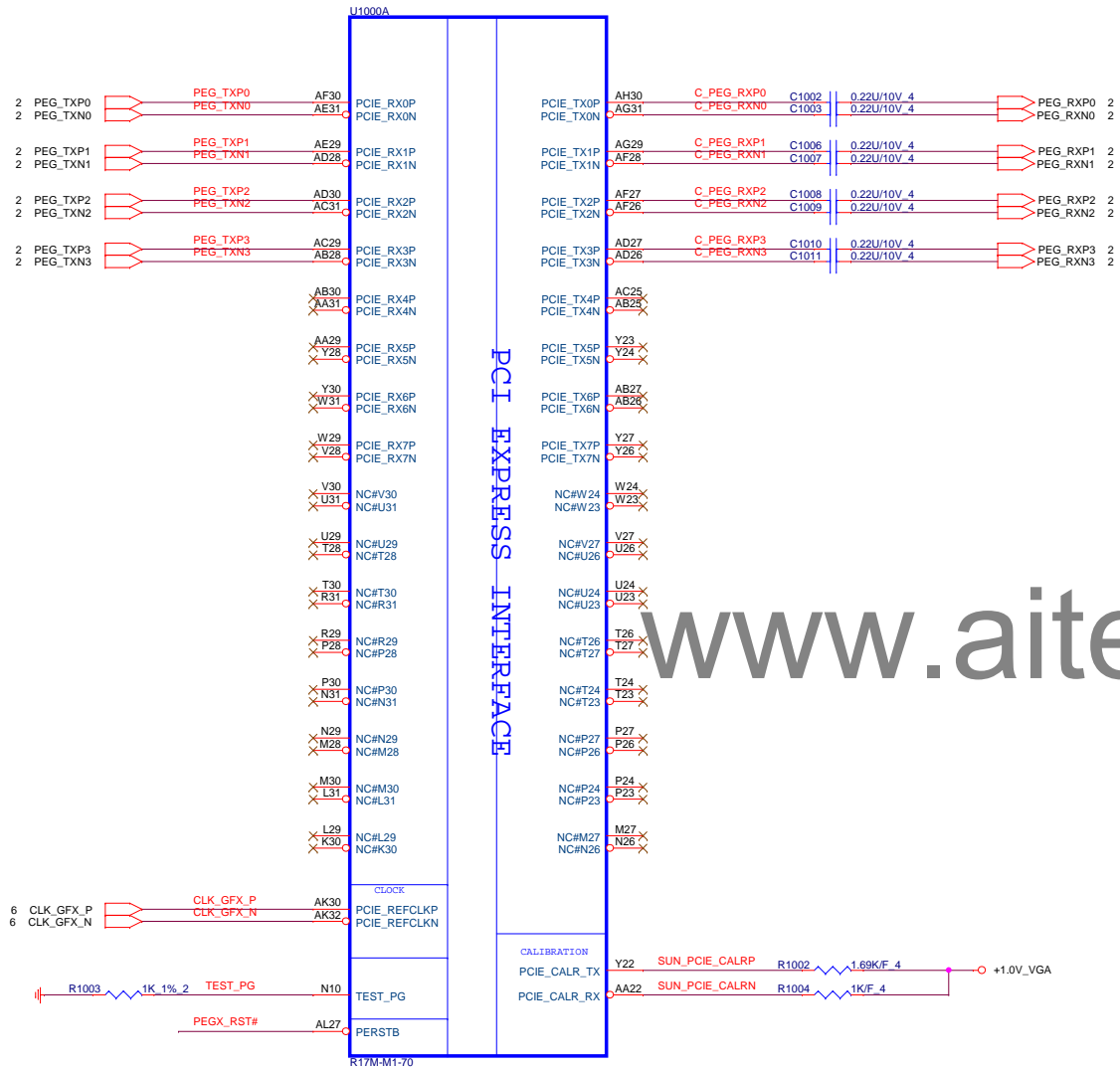
Main:AL000781039	G781-1P8(9Ah)
2nd:AL001412005	EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003	EMC1412-1-ACZL-TR(98h)
2nd:AL000431014	TMP431ADGKR(98h)



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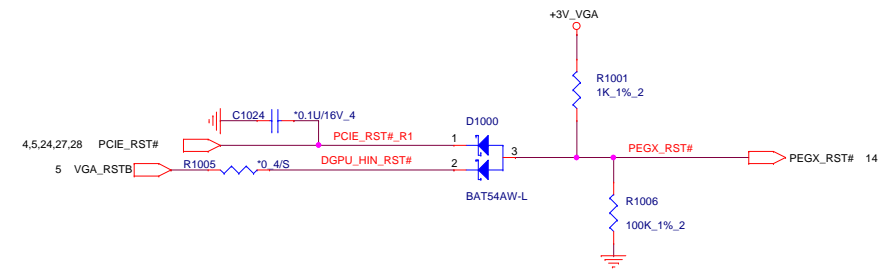
 NB5	<b>PROJECT:NFLP-G94A</b>		
	Quanta Computer Inc.		
	Size C	Document Number Reserved	Rev 1A
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14,16,43,44,47 +3V\_VGA  
14,16,43,44,47 +1.8V\_VGA  
16,43,47 +1.0V\_VGA



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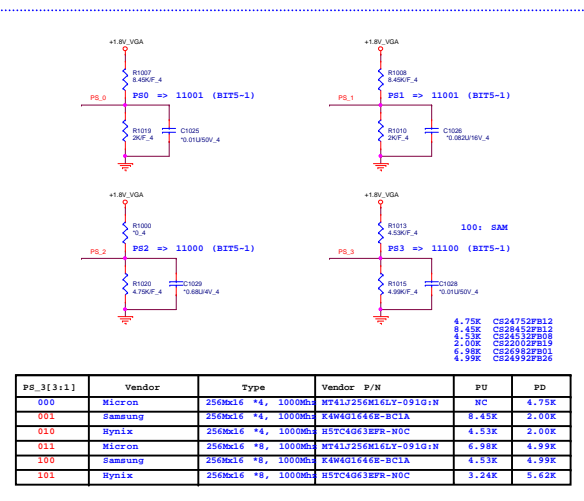
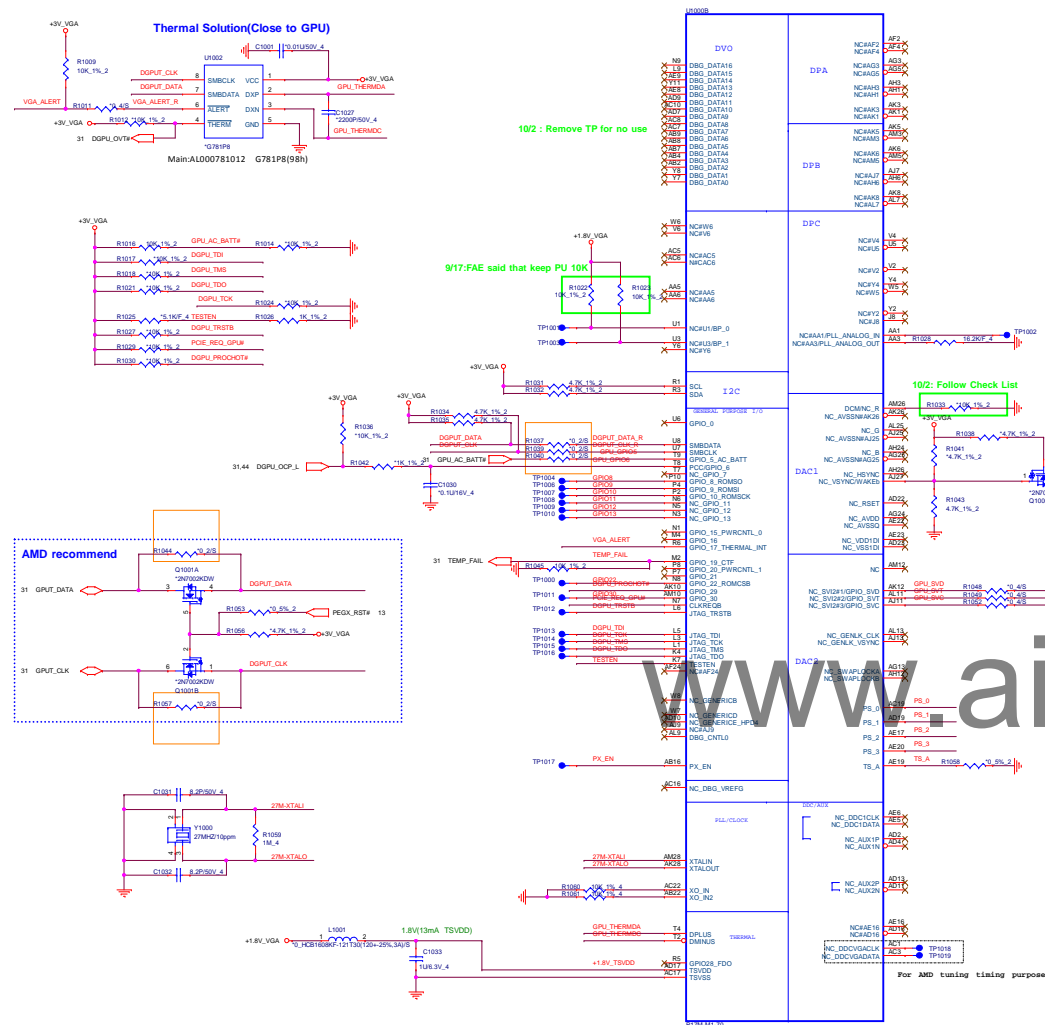
#### GPU Reset Signal



**PROJECT:NFLP-G94A**

**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>M1-70_S3_PCIE/DP POWER</b>	1A
Date: Monday, January 16, 2017	Sheet	13 of 48



PS PS Implementation

- Connect GPD\_2B to 10K pull-down to enable HUPs
- Pin of PS\_0 (U12) is not used, leave "No connect"
- R, pu, R, pd and C must be properly populated per tables below
- PS pin must connect to the PS pin and C should be less than 2 ohms
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Load Table

C (pF)	Resistor (Ohm)	R, pu (Ohm)	R, pd (Ohm)	Cap (pF)
000	NC	4750	000	000
01	01	8450	000	000
10	10	4530	2000	000
NC	11	6980	8990	001
		4530	4990	100
		3240	5620	101
		3400	10000	110
		4750	NC	111

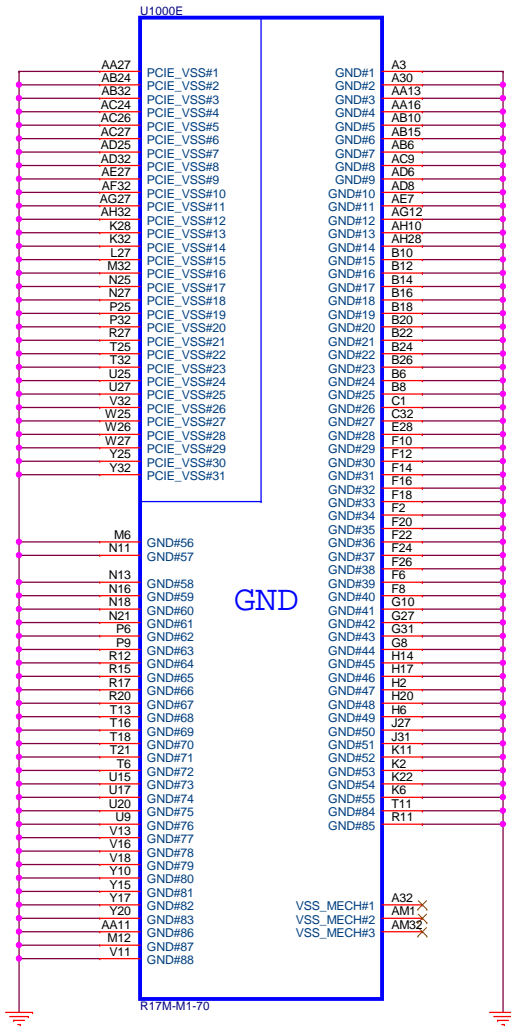
Resistor Divider Loading Table

R, pu (Ohm)	R, pd (Ohm)	Cap (pF)
NC	4750	000
8450	000	000
4530	2000	000
6980	8990	001
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Table 3-24 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

NFLP Bit	Strap Name	Description	Recommended Settings
PS_H01	ROM_CONFIG[0]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[0] follows the BIOS type.	Design dependent, use the description.
PS_H02	ROM_CONFIG[1]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[1] follows the primary memory aperture size. See Table 3-24 Primary Memory Aperture Size.	Design dependent, use the description.
PS_H03	ROM_CONFIG[2]	Reserved for internal use only. Must be 1 at reset.	1
PS_H04	N/A	Reserved.	1
PS_H05	N/A	Reserved.	1
PS_H10	STRAP_BIF_GEN0_EN_A	1 = PCIe GEN3 capabilities. 0 = PCIe GEN3 is not supported.	Design dependent, use the description.
PS_H20	STRAP_BIF_CLK_PEN	1 = The CLKREQ# power management capability is disabled. 0 = The CLKREQ# power management capability is enabled.	0
PS_H30	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_H40	STRAP_TX_CFG_DRV_FULL_SWING	1 = The transmitter full-swing is enabled. 0 = The transmitter full-swing is disabled.	1
PS_H50	STRAP_TX_DEEMPH_PEN	PCI EXPRESS#8 transmitter, de-emphasis enabled. 0 = Tx de-emphasis disabled. 1 = Tx de-emphasis enabled.	Design dependent, use the description.
PS_H60	N/A	Reserved.	0
PS_H70	N/A	Reserved.	0
PS_H80	STRAP_BIOS_ROM_EN	1 = Enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device.	Design dependent, use the description.
PS_H90	N/A	Reserved.	0
PS_HA0	N/A	Reserved.	0
PS_HB0	BOARD_CONFIG[0]	Board configuration related information, such as memory ID.	Design dependent, use the description.
PS_HC0	BOARD_CONFIG[1]	Board configuration related information, such as memory ID.	Design dependent, use the description.
PS_HD0	N/A	Reserved.	0
PS_HE0	N/A	Reserved.	0



# **CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS** **ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED,** **THEY MUST NOT CONFLICT DURING RESET**

RECOMMENDED SETTINGS  
 0= DO NOT INSTALL RESISTOR  
 1 = INSTALL 3K RESISTOR  
 X = DESIGN DEPENDANT  
 NA = NOT APPLICABLE

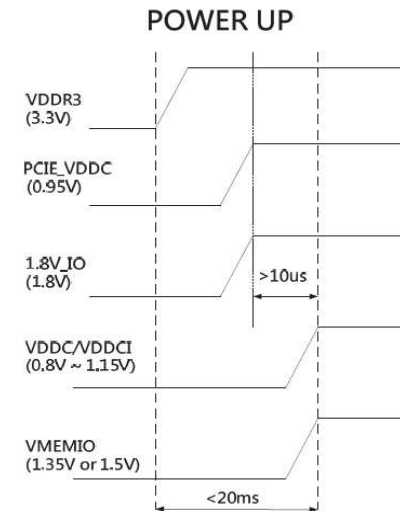
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYSN	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

## **NOTE1: AMD RESERVED CONFIGURATION STRAPS**

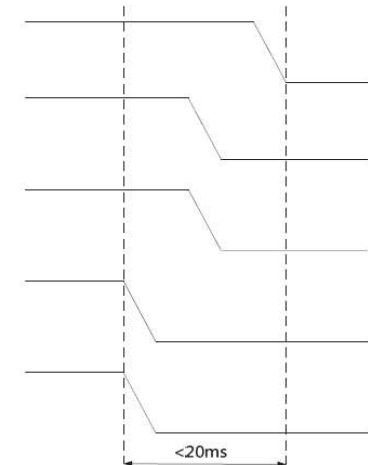
**ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.**

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

## **POWER UP / POWER DOWN SEQUENCE**



## **POWER DOWN**

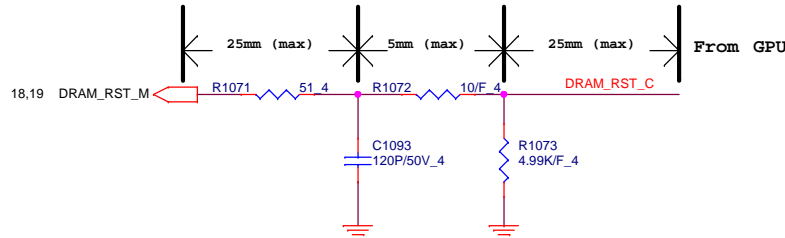
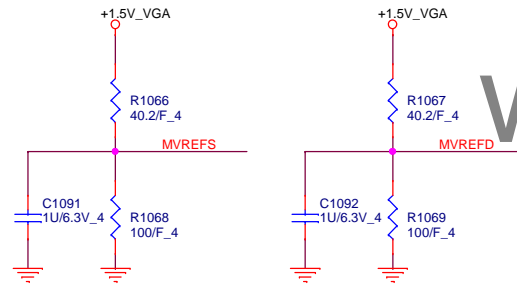
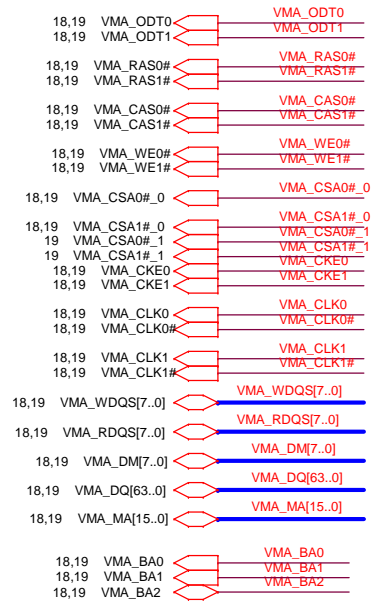


**PROJECT:NFLP-G94A**

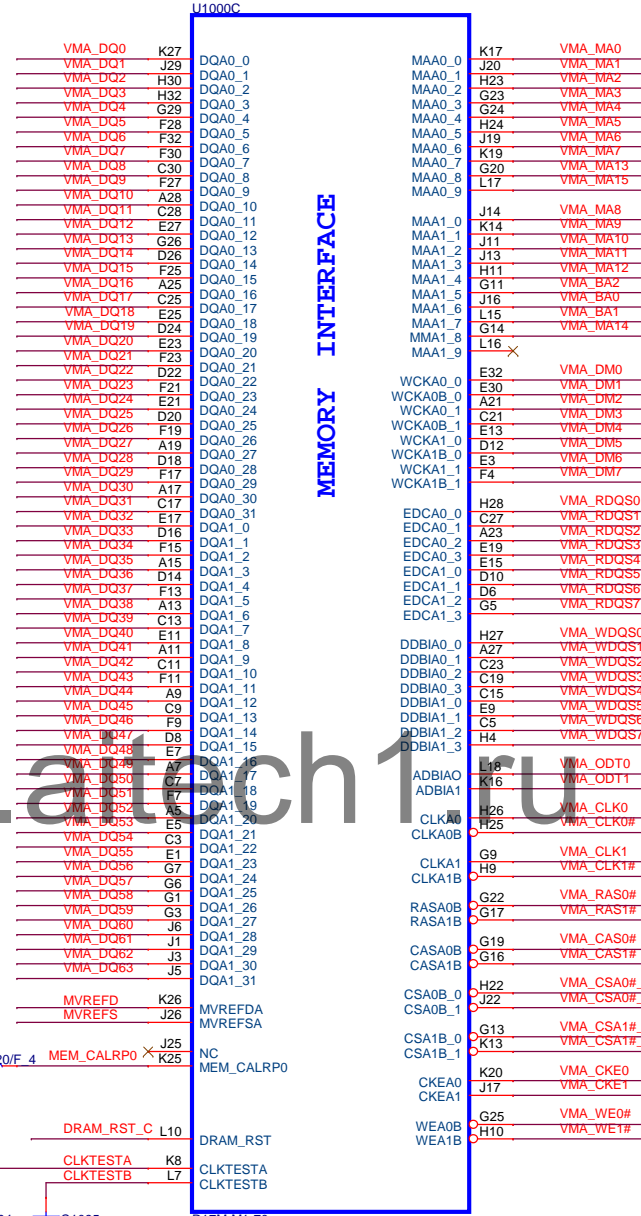
**Quanta Computer Inc.**

Size	Document Number	Rev
M1-70_S3_GND/LVDS/Strap		1A
Date:	Monday, January 16, 2017	Sheet 15 of 48

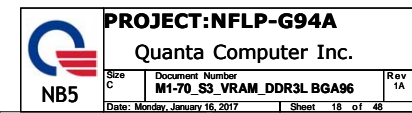




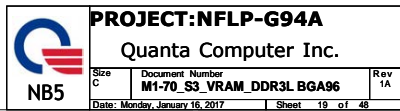
Place all these components very close to GPU. (Within 25mm)  
Keep all component close to each Other. (within 5mm)  
This basic topology should be used for DRAM\_RST for DDR3/GDDR5.



16,18,19,43,46 +1.5V\_VGA



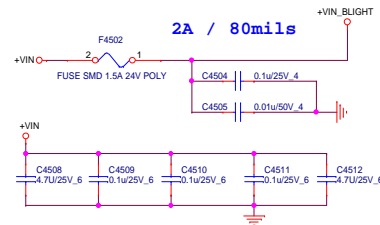
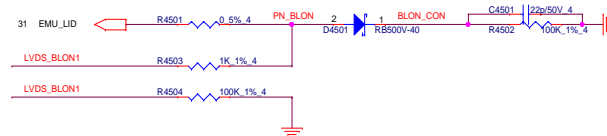




**FP is ok, PN wait confirm**

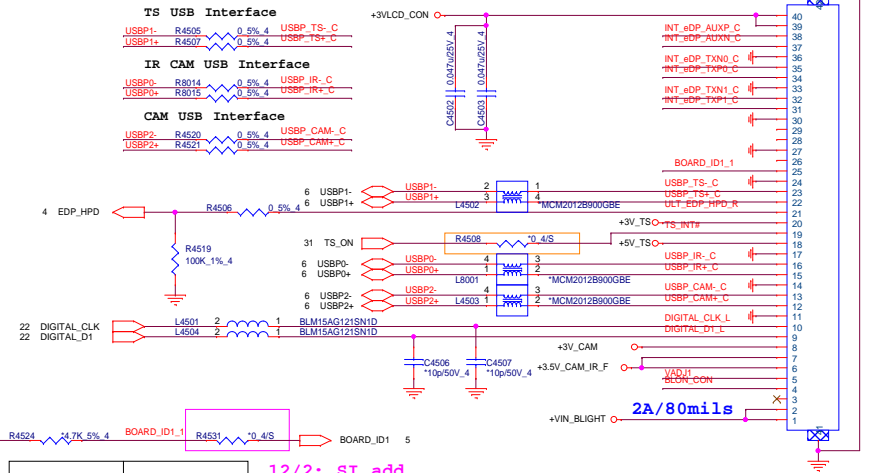
GS12401-1011-0H  
51519-04007-V02-40P-L

## LID Switch



## eDP CONN

**TS USB Interface**  
 USBP1- R4505 0.5% 4 USBP\_TS- C  
 USBP1+ R4507 0.5% 4 USBP\_TS+ C  
**IR CAM USB Interface**  
 USBP0- R8014 0.5% 4 USBP\_IR- C  
 USBP0+ R8015 0.5% 4 USBP\_IR+ C  
**CAM USB Interface**  
 USBP2- R4520 0.5% 4 USBP\_CAM- C  
 USBP2+ R4521 0.5% 4 USBP\_CAM+ C

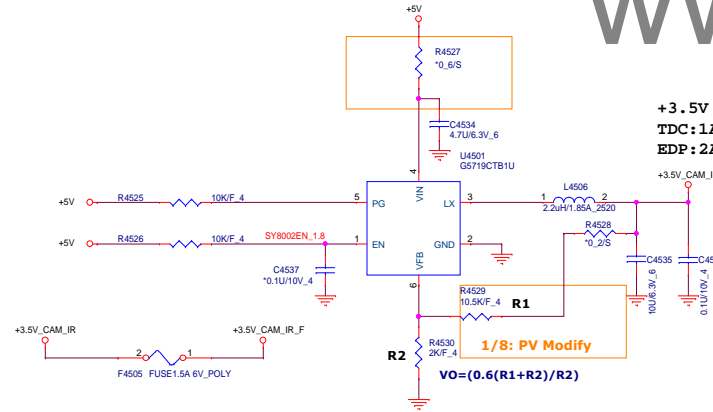


TP_ID	Definition
0	14* 17*
1	15*

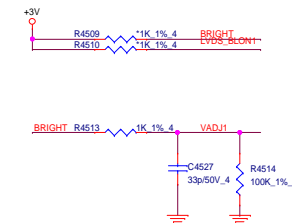
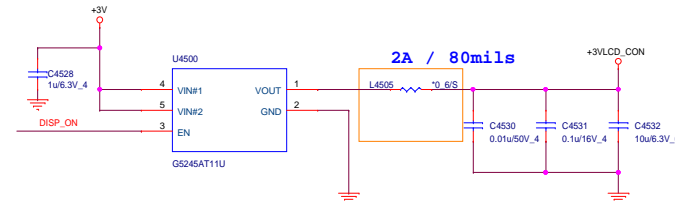
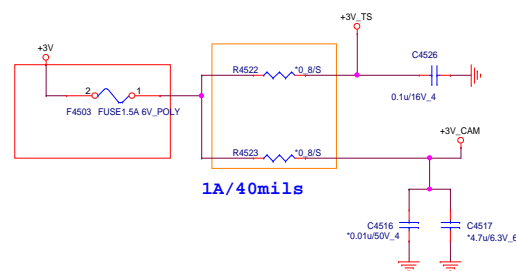
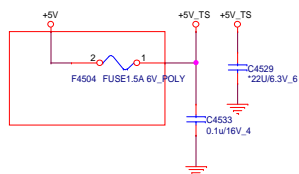
12/2: SI add

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**+3.5V +/- 5%**  
**TDC:1A**  
**EDP:2A**

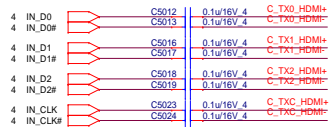


## Touch screen

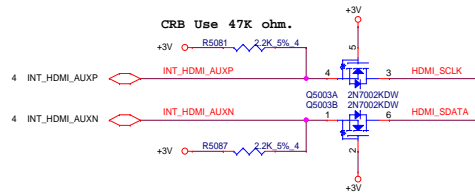


**Need change DK150TPU018**

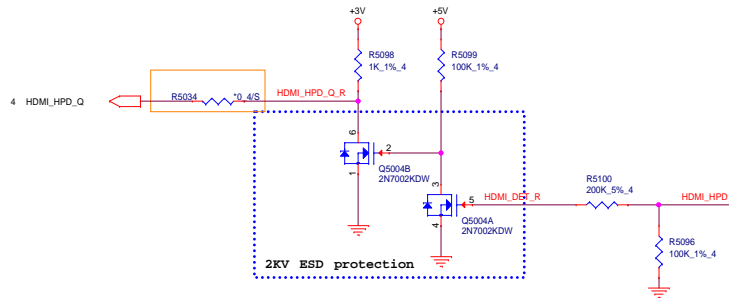
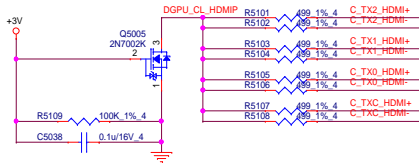
## HDMI CONN



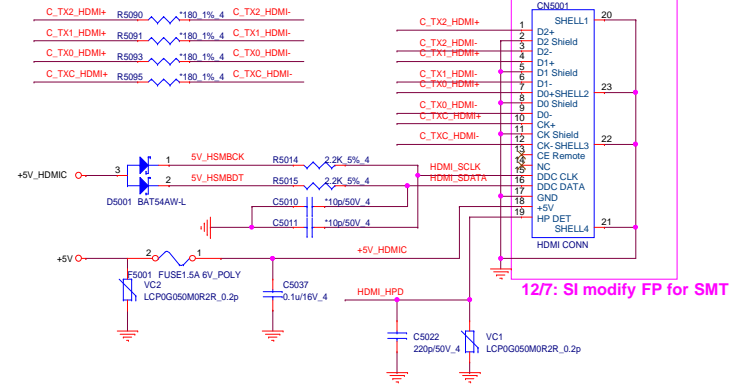
## HDMI SMBus isolation



**Close to HDMI connector**



For EMI Solution

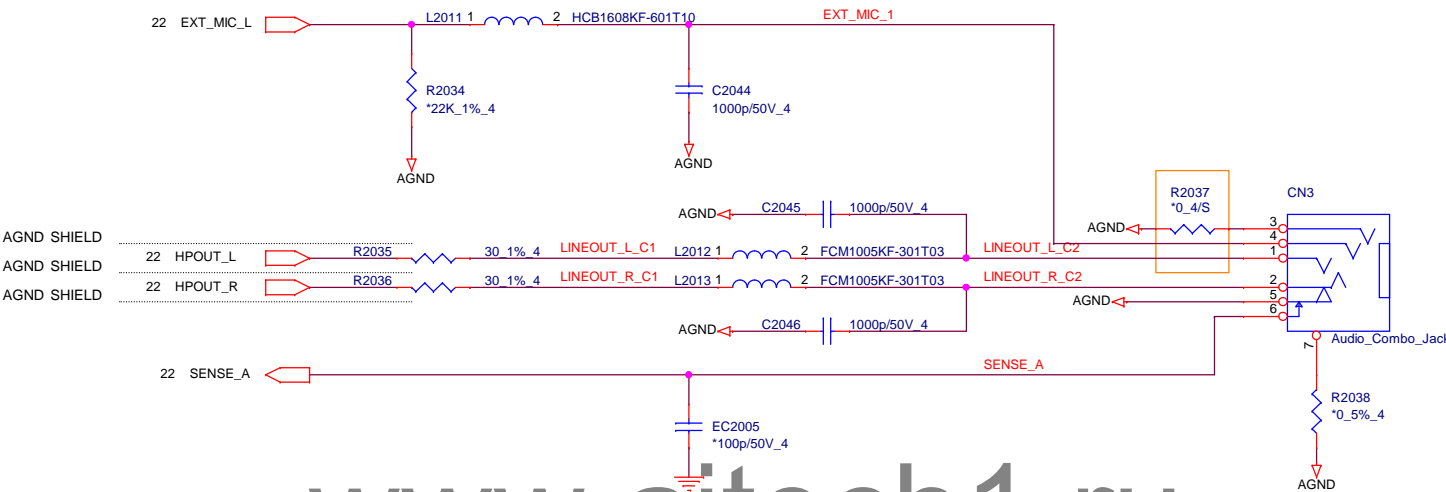


For ESD Solution

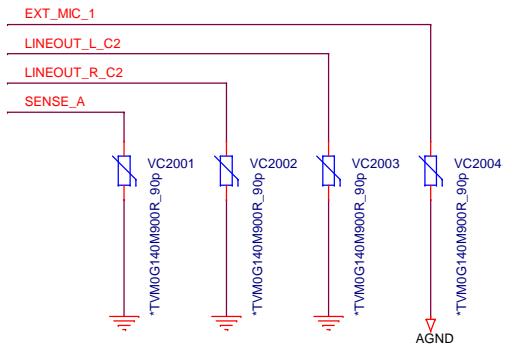


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Audio JACK ESD

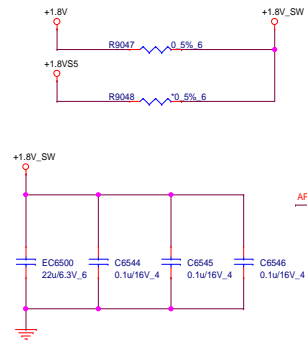
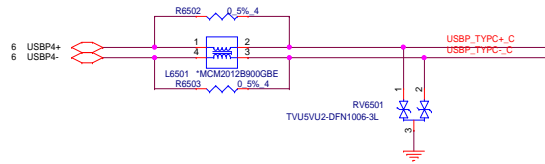


 NB5	<b>PROJECT:NFLP-G94A</b>		
	Quanta Computer Inc.		
	Size B	Document Number <b>Audio Jack</b>	Rev 1A
Date: Monday, January 16, 2017			Sheet 23 of 48



# USB3 SW - PI2EQX632 + USB TYPE-C - TPS25810

## USB2.0

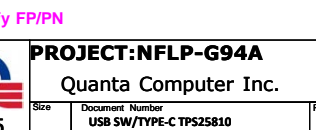
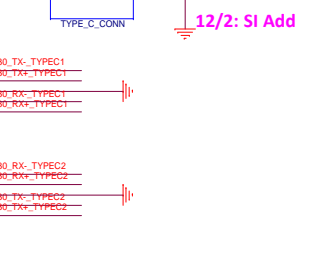
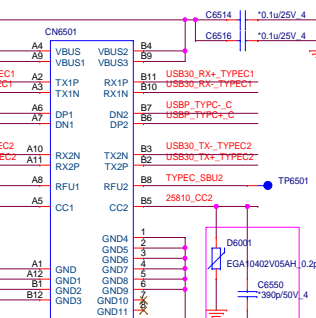
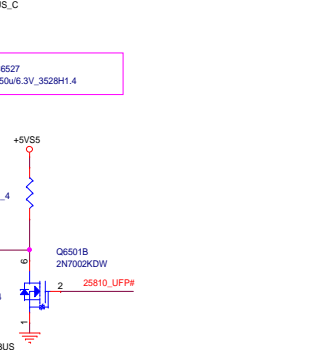
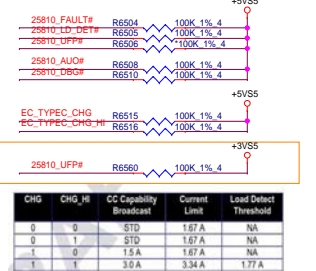
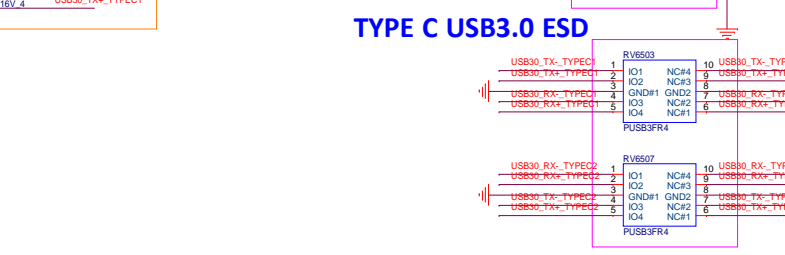
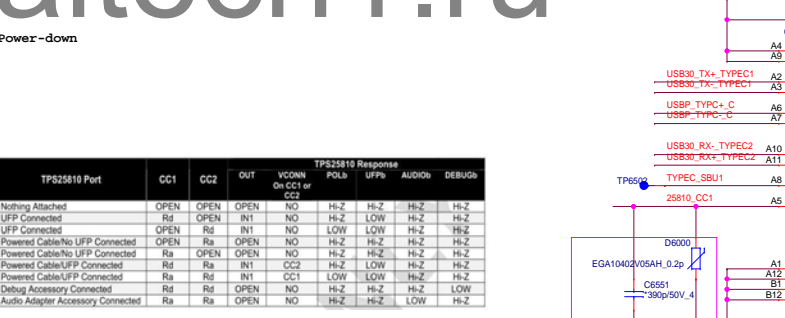
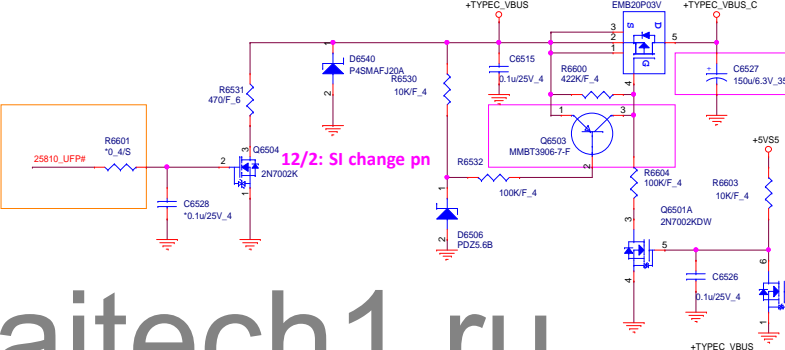
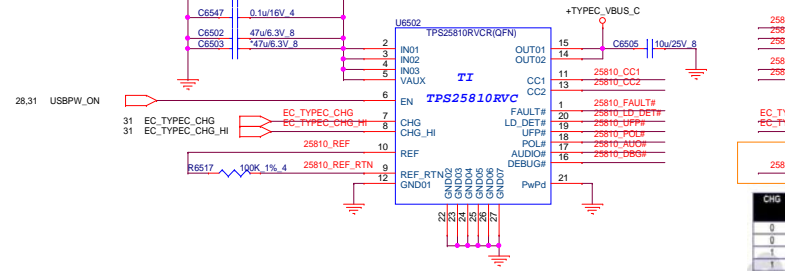
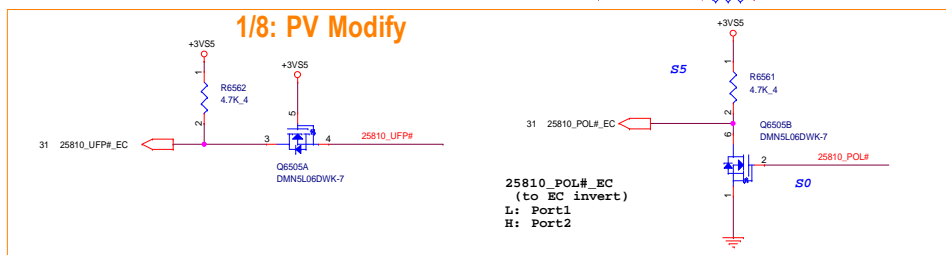


11/27: SI change Pin define & Symbol error

## USB3.0 SW

12/6: SI change U6501 FP for SMT

1/8: PV Modify

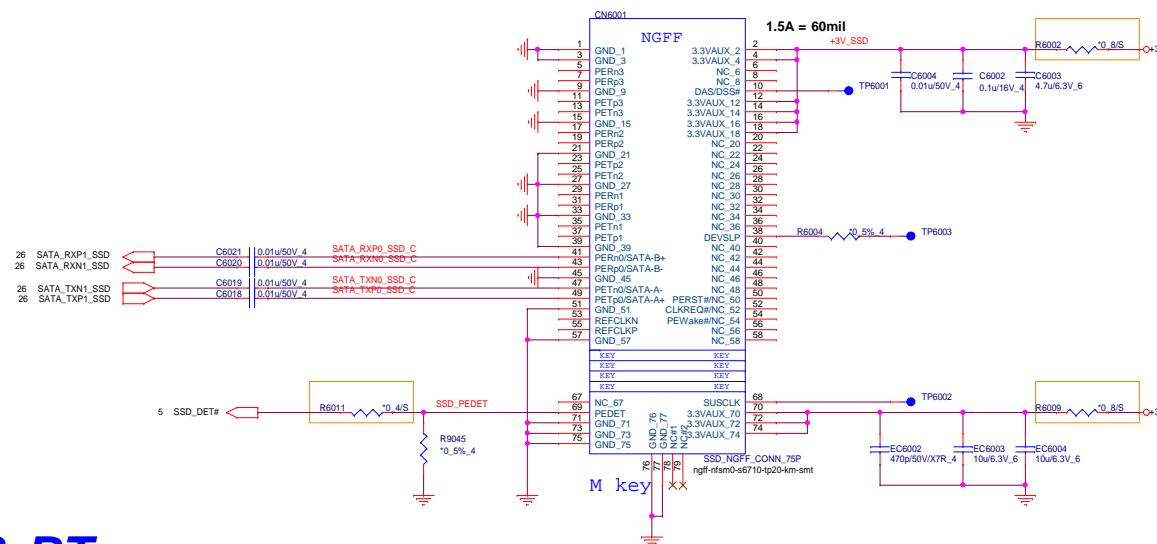




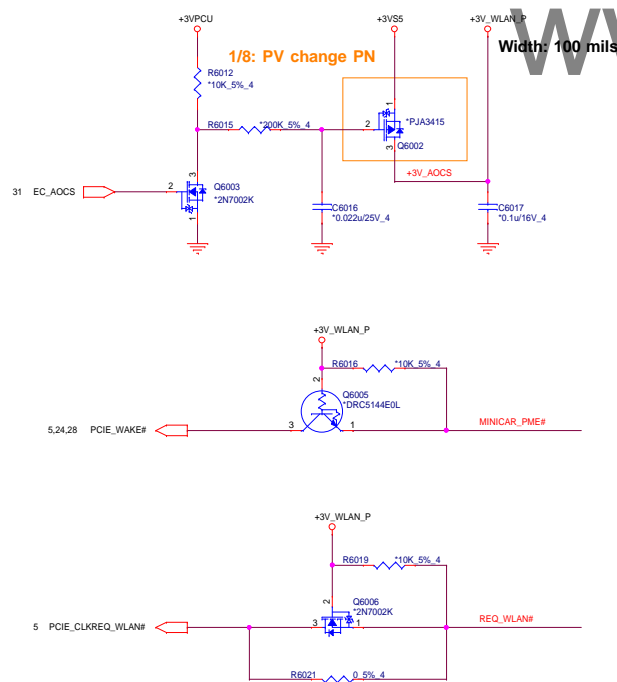


## SATA SSD

Conn PN FP OK! Libray modify, add Pin78,79

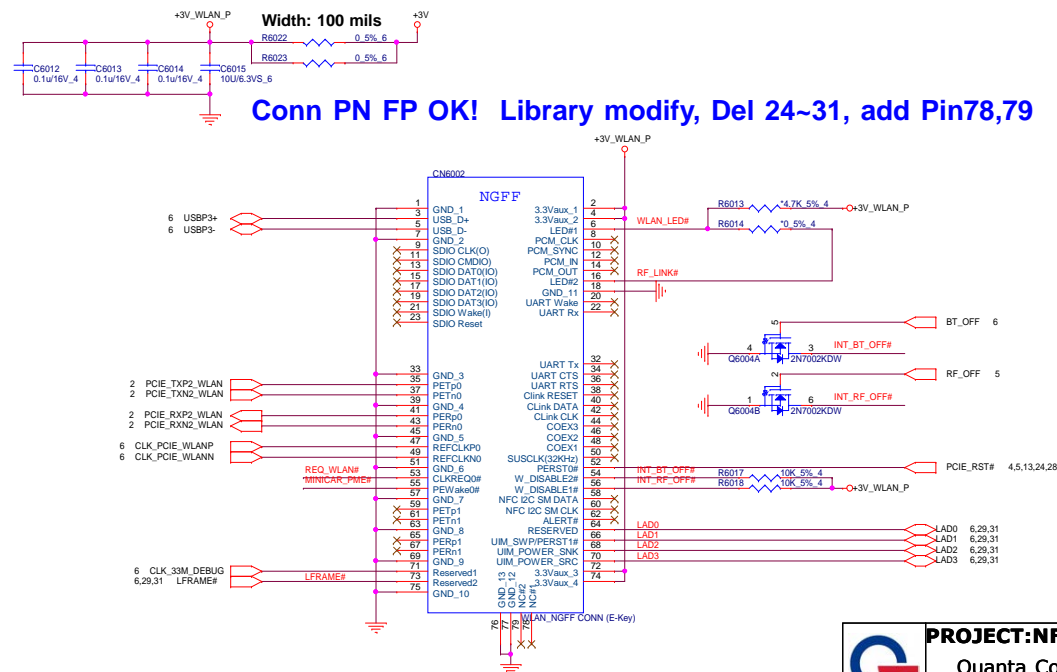


## WLAN & BT



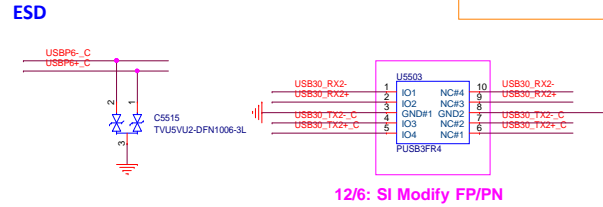
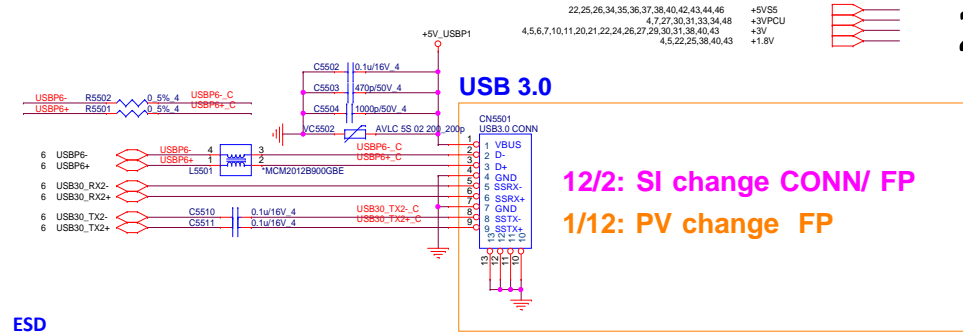
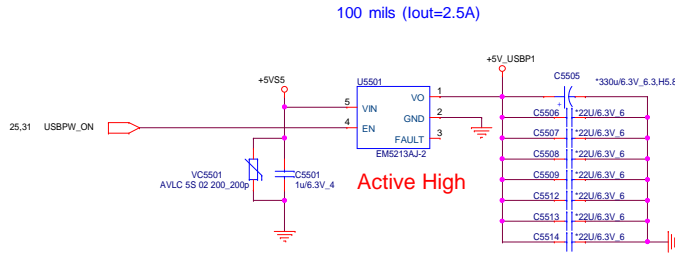
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Conn PN FP OK! Library modify, Del 24~31, add Pin78,79



For 15.6" / 17.3" 2SPD

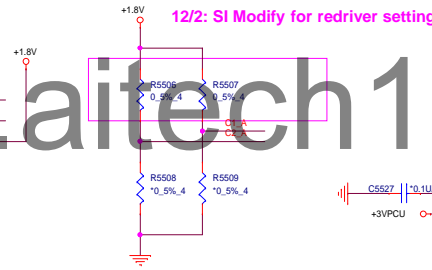
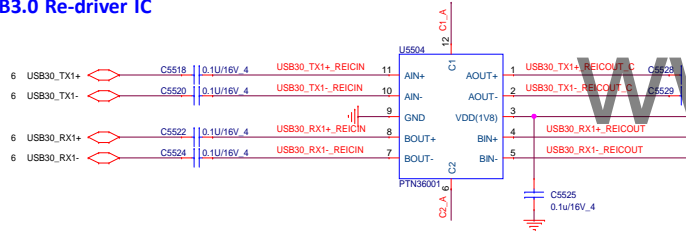
28



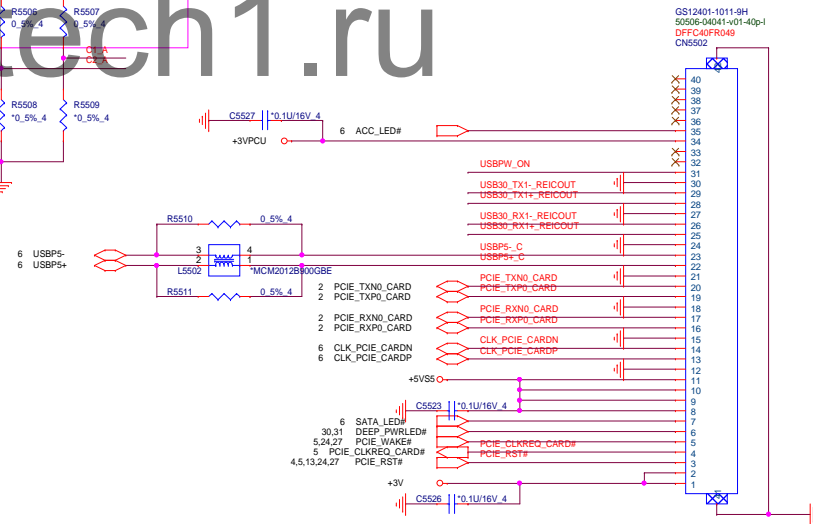
## USB3.0

USB3.0 Re-driver IC

USB3.0 re-driver IC

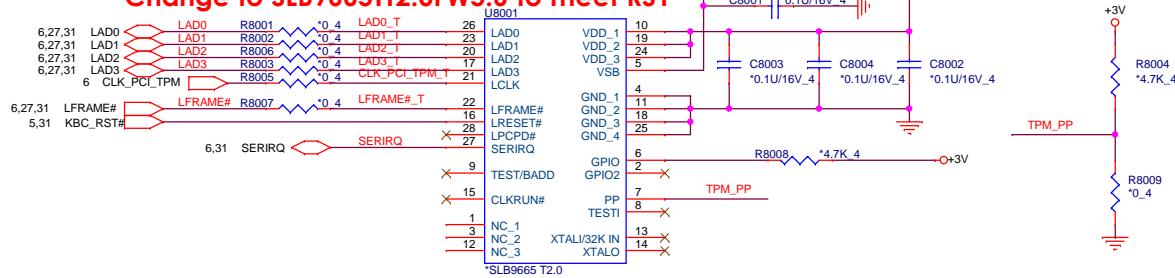


Confirm Library!



## TPM (2.0)

Change to SLB9665T2.0FW5.6 to meet RS1



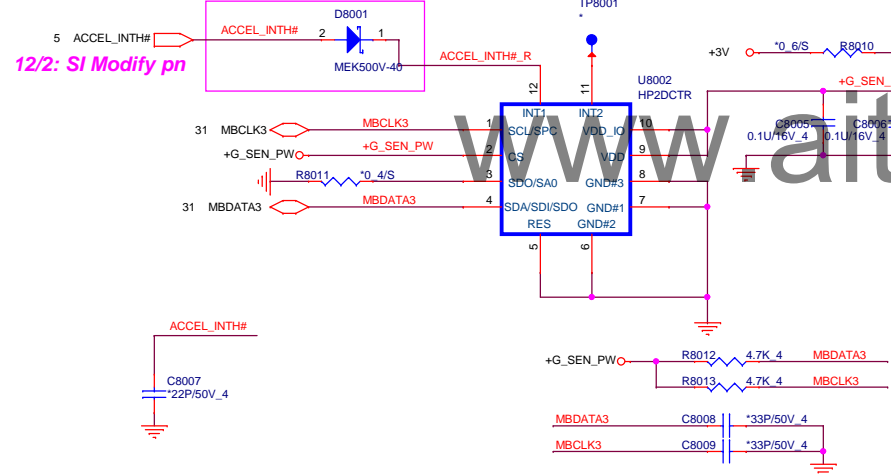
4,5,6,7,10,11,20,21,22,24,26,27,28,30,31,38,40,43

+3V\_WLAN\_P  
+3V



29

## Accelerometer Sensor

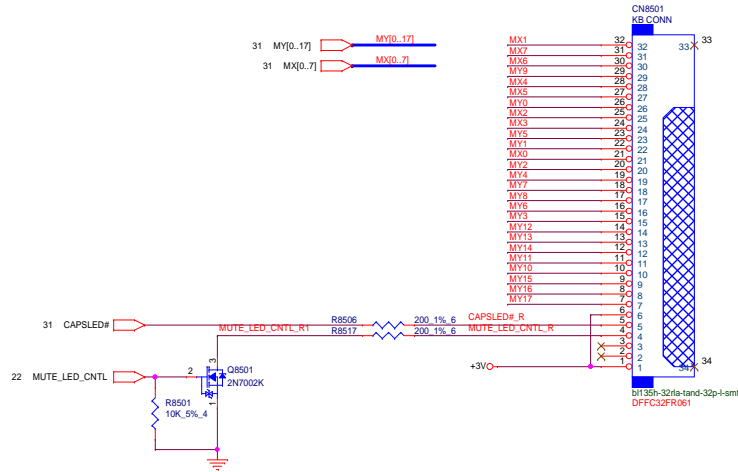


IR CAM on Page20

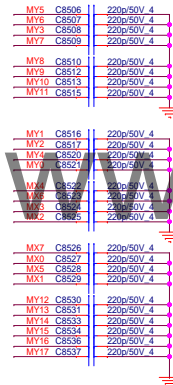
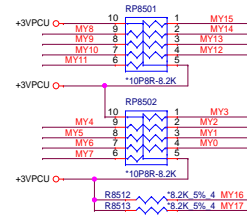
# KEYBOARD CONN

Conn Wait confirm FP!!

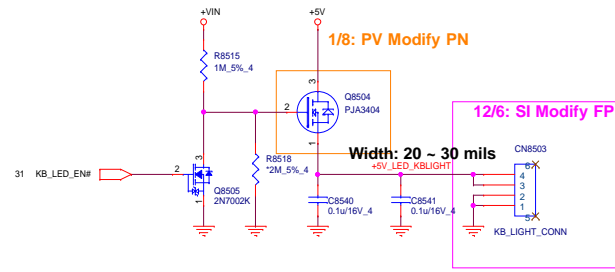
# Touch Pad CONN



## KEYBOARD PULL-UP

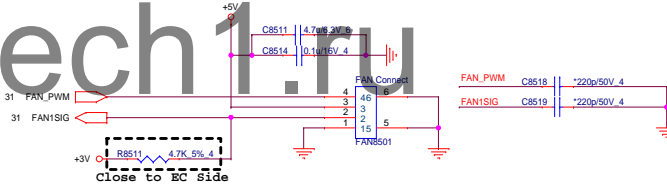


# KB LIGHT CONN



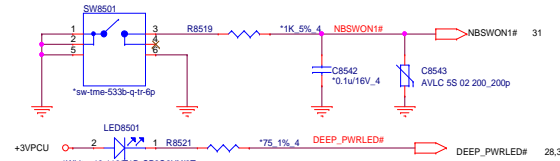
# FAN CONN

confirm Library

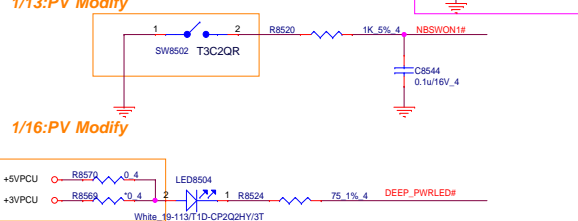


# PWR Button & LED & HALL IC

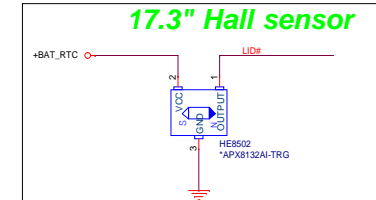
## 17.3" SW & LED



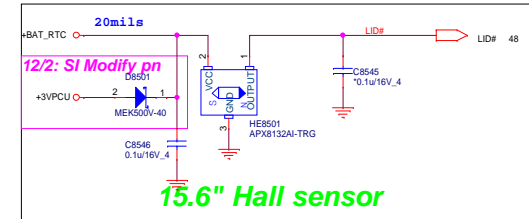
## 15.6" SW & LED

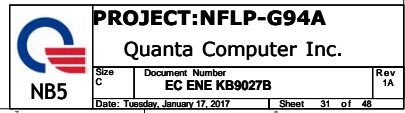
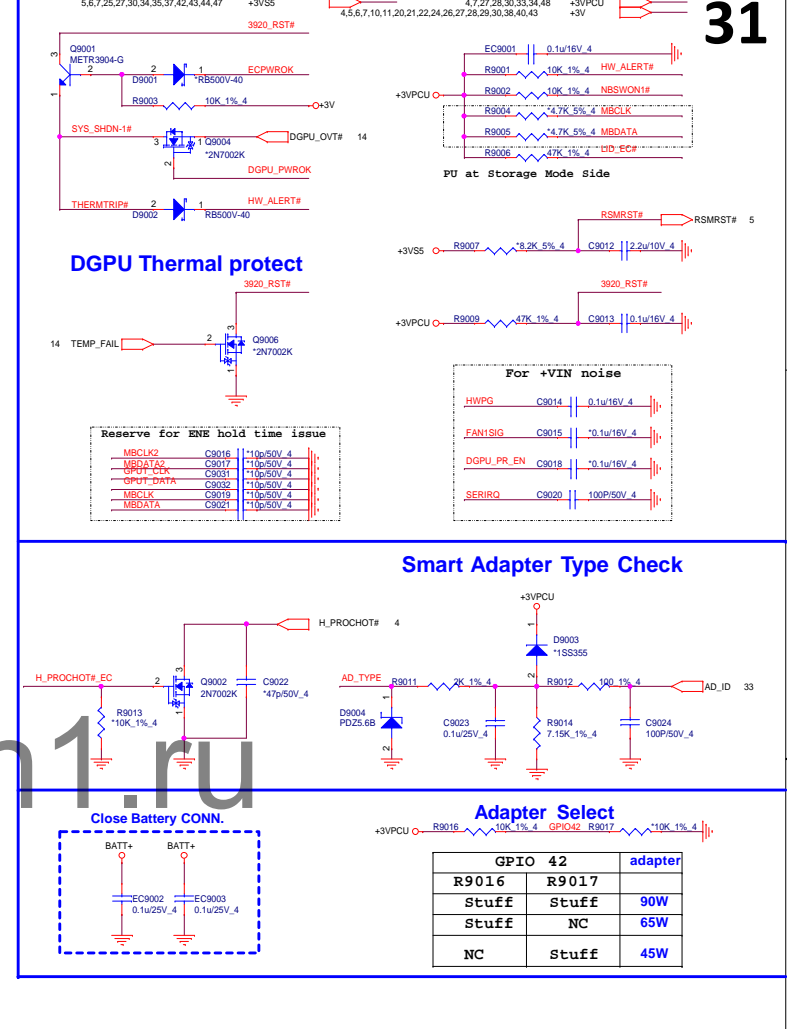


## 17.3" Hall sensor



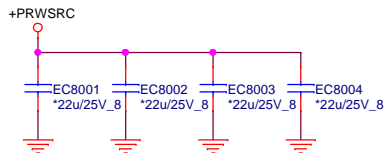
## 15.6" Hall sensor



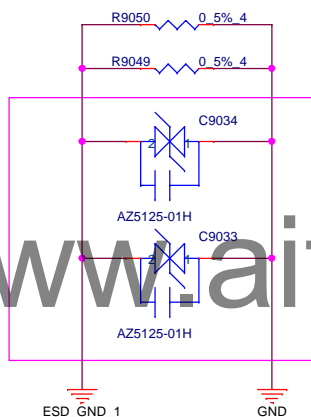
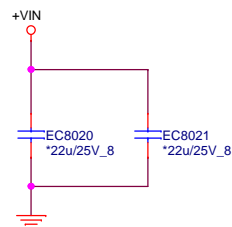
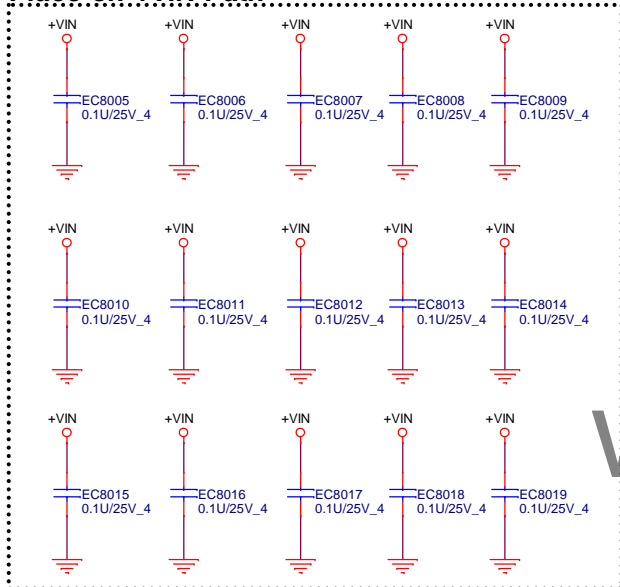


# EMI CAPs

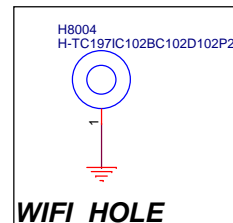
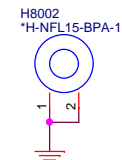
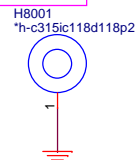
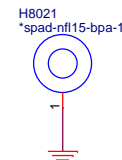
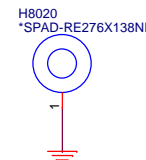
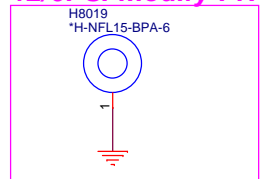
## For ISN



## Place on +VIN Path

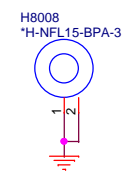
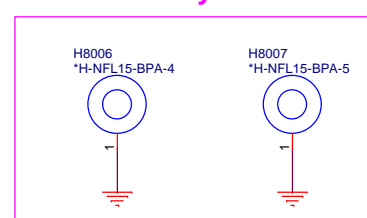


## 12/6: SI modify PN

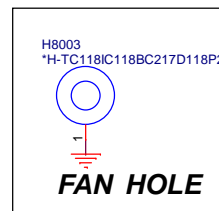
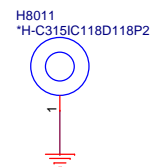
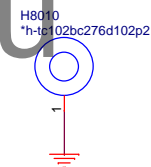
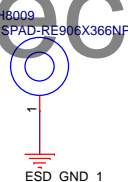


WIFI HOLE

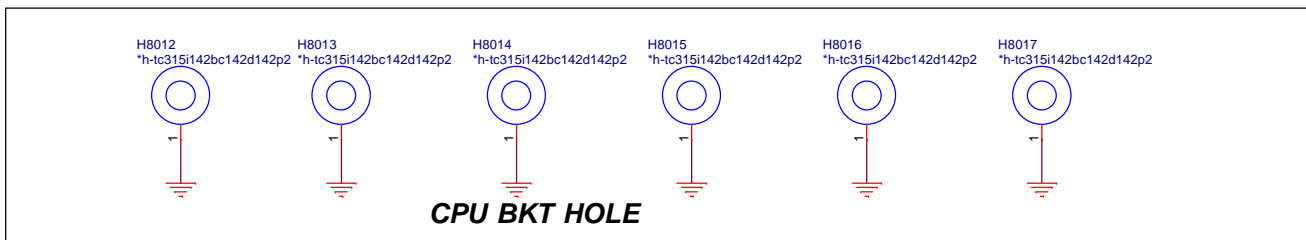
## 12/6: SI modify PN



## 12/2: SI modify PN



FAN HOLE



CPU BKT HOLE



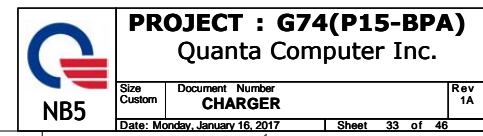
PROJECT:NFLP-G94A

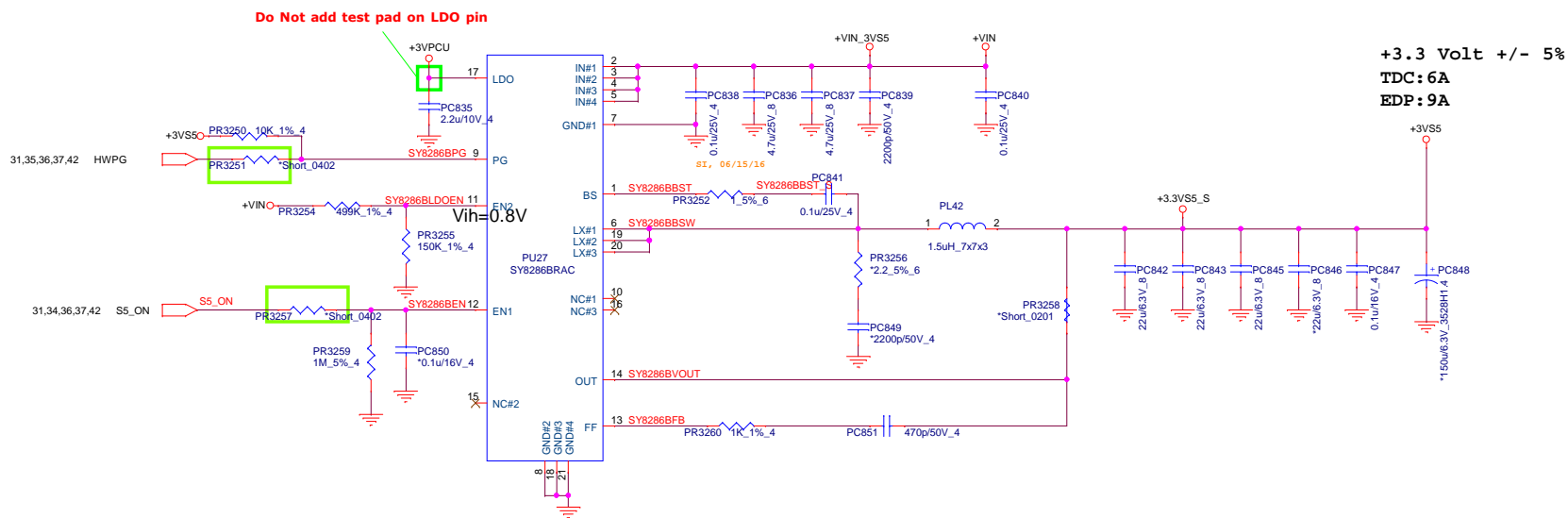
Quanta Computer Inc.

Size B	Document Number	Rev 1A
	EMI CAP/HOLES	
Date: Monday, January 16, 2017	Sheet 32 of 48	

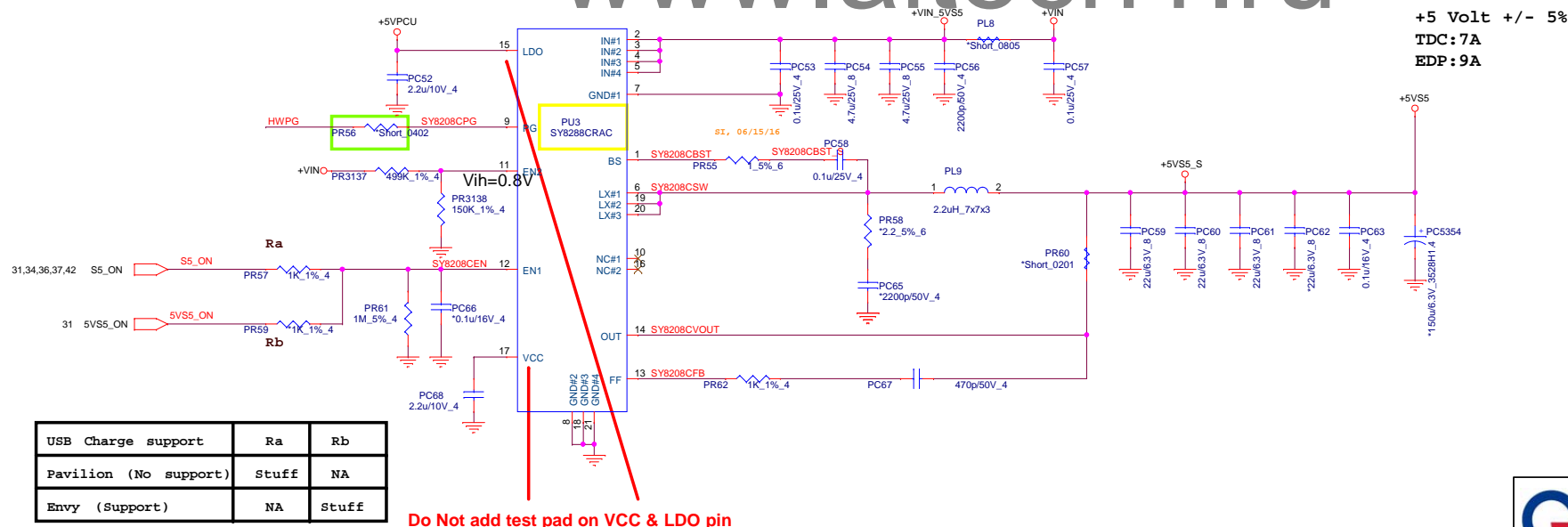


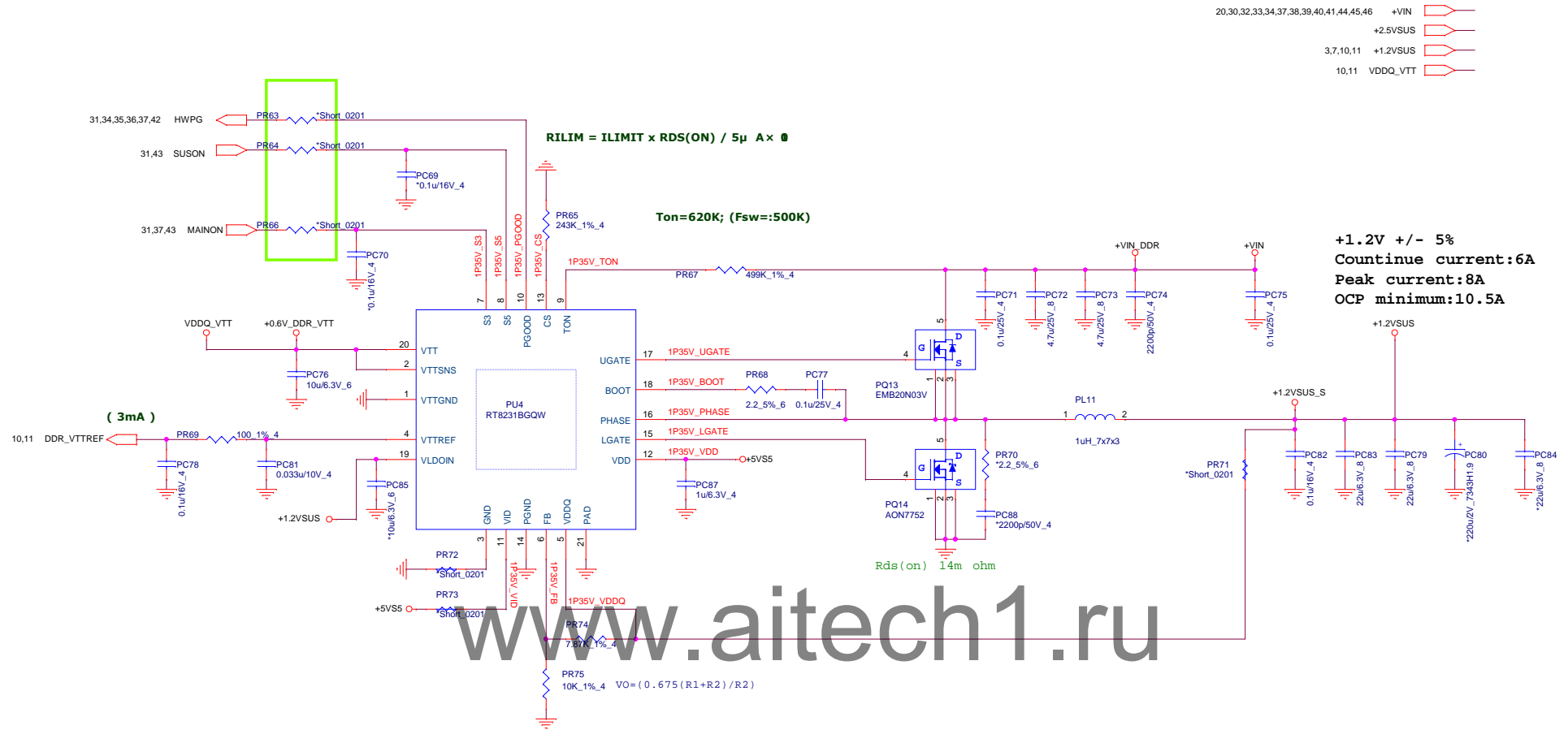
**Do Not add test pad on BQBATDRV/BATDIS\_ID\_DOD signal**

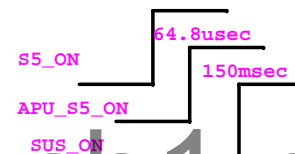
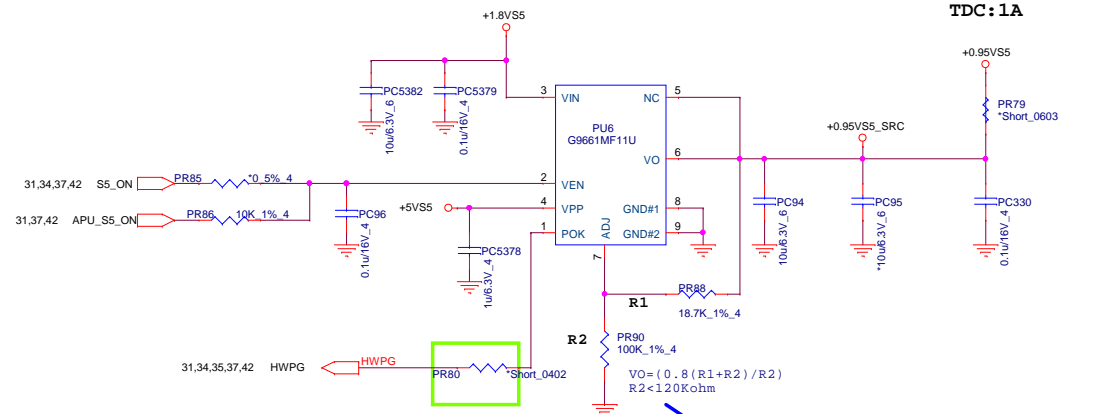




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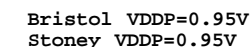




	R1		
Stoney/Bristol	18.7K	CS31872FB19	0.95V
	31.6K	CS33162FB14	1.05V

Bristol VDDP=1.05V  
Stoney VDDP=0.95V

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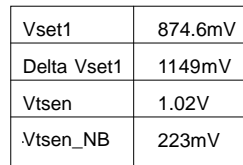


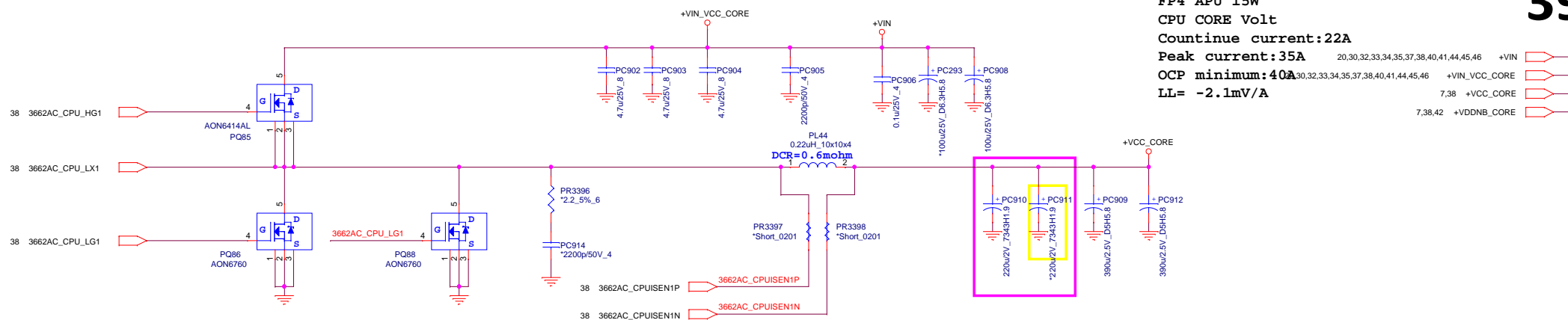
Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

	R1		
Stoney / Bristol	1.91K	CS21912FB13	0.95V
	3.16K	CS23162FB04	1.05V

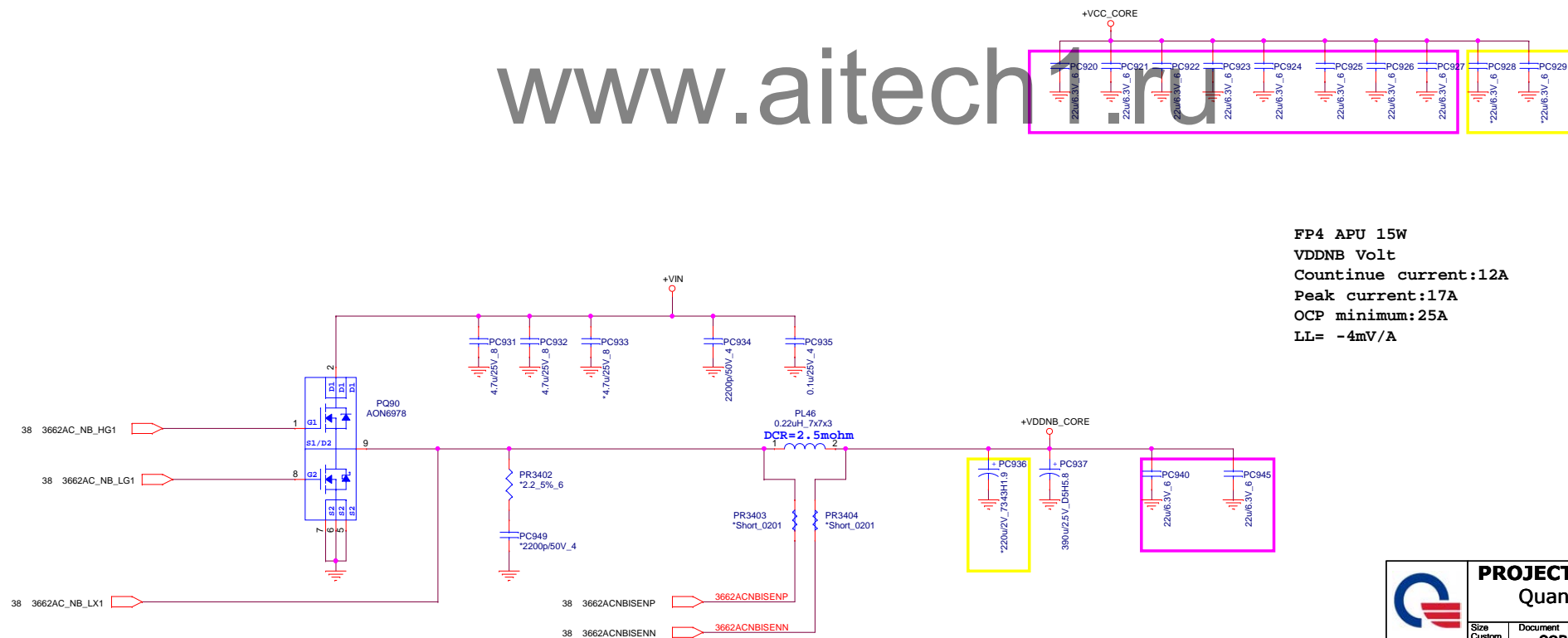
[illegible]

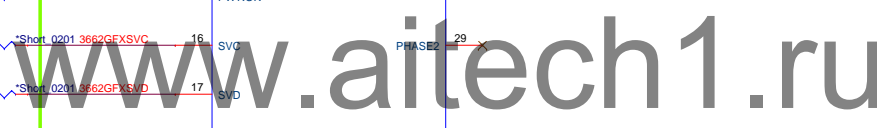
$$V_0 = 0.6 * (R_1 + R_2) / R_2$$





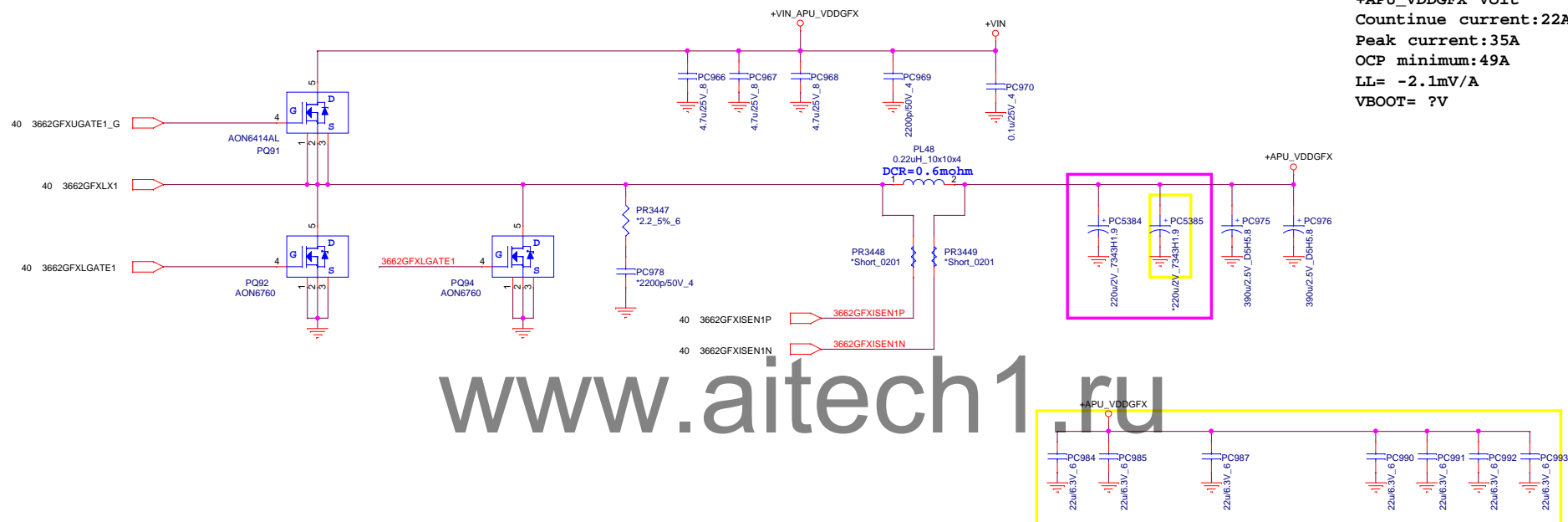
www.aitech.ru



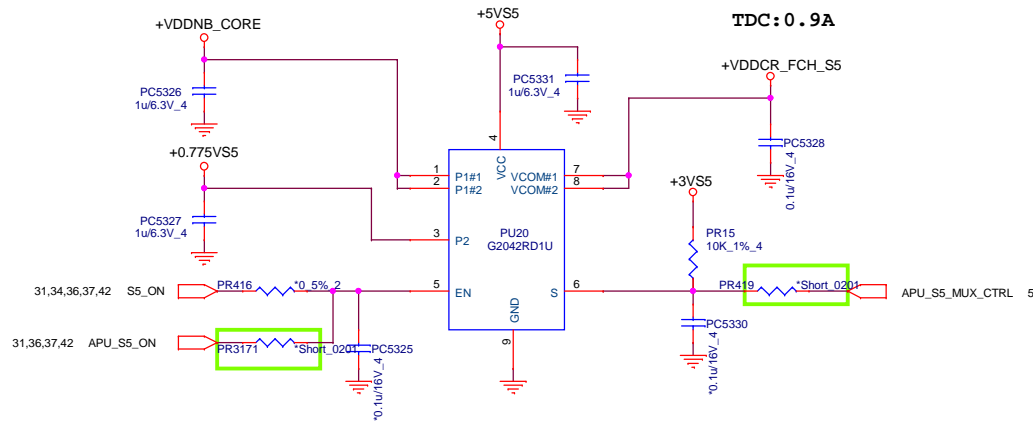




CPU	Page 40 & Page 41
Bristol	Stuff
Stonley FP4,FT4	Unstuff

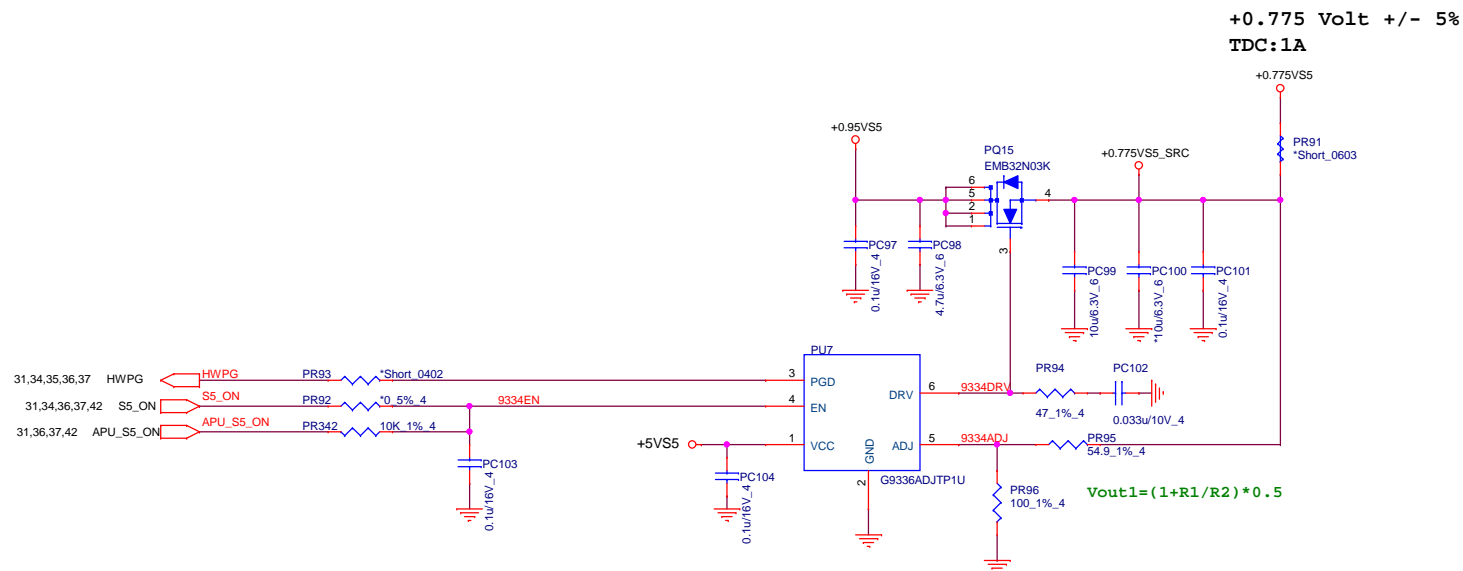


```
+APU_VDDGFX Volt
Continue current:22A
Peak current:35A
OCP minimum:49A
LL= -2.1mV/A
VBOOT= ?V
```



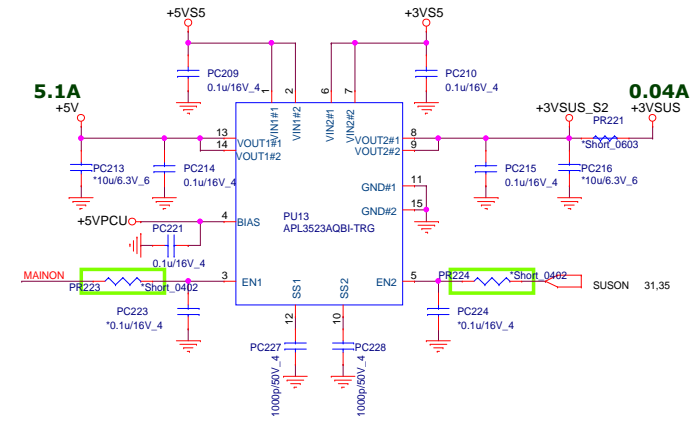
EN	SEL	VIN1	Vo
0	X	0.775V~1.2V	0V
1	0	<0.775V	0.775V
1	0	>0.775V	VDDNB
1	1	0.775V~1.2V	VDDNB

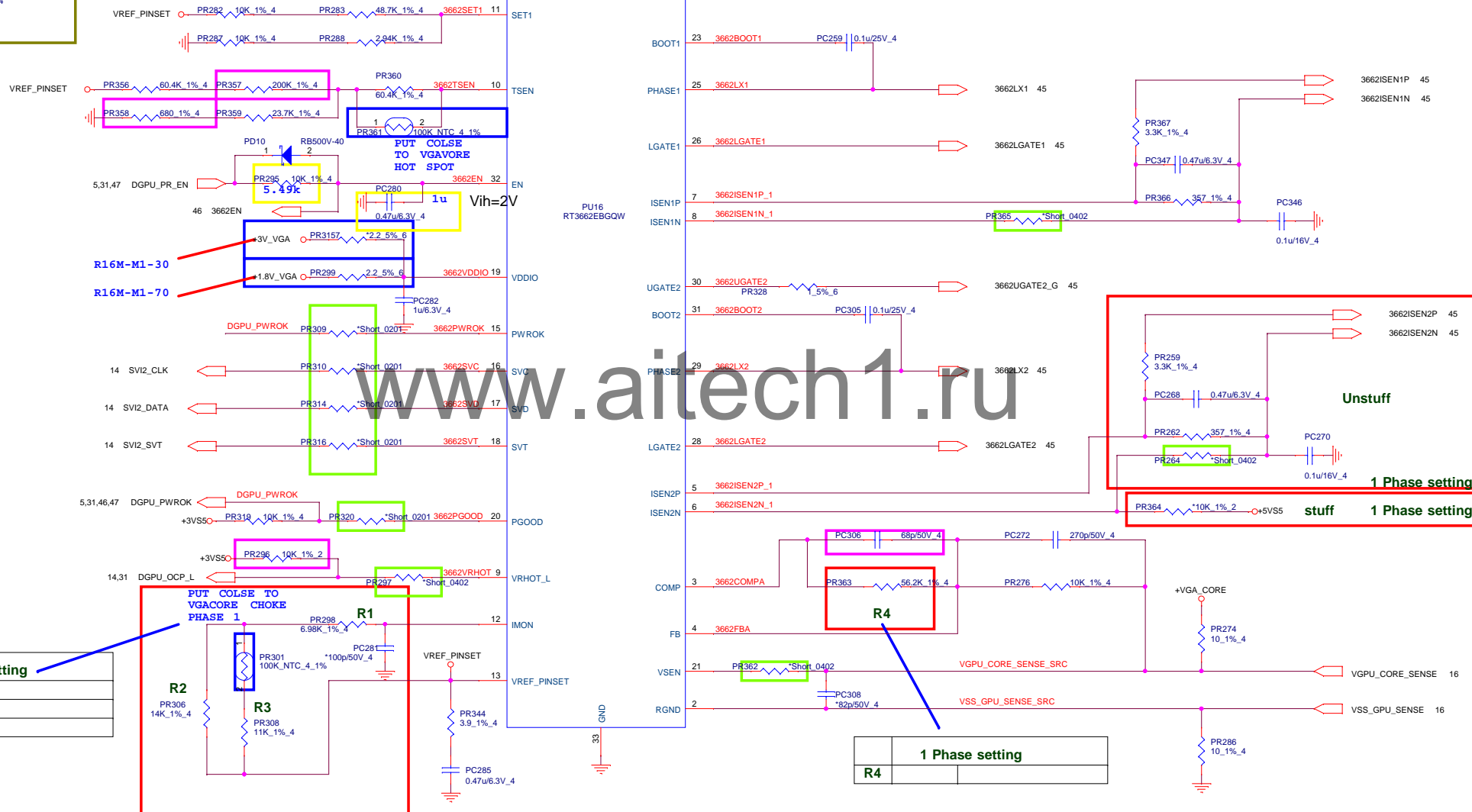
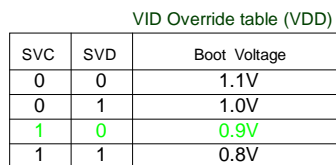
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**PROJECT : G74(P15-BPA)**  
Quanta Computer Inc.


Size	Document Number	Rev
Custom	VDDCR_FCH/0.775VS5	1A
Date: Monday, January 16, 2017	Sheet 42 of 48	

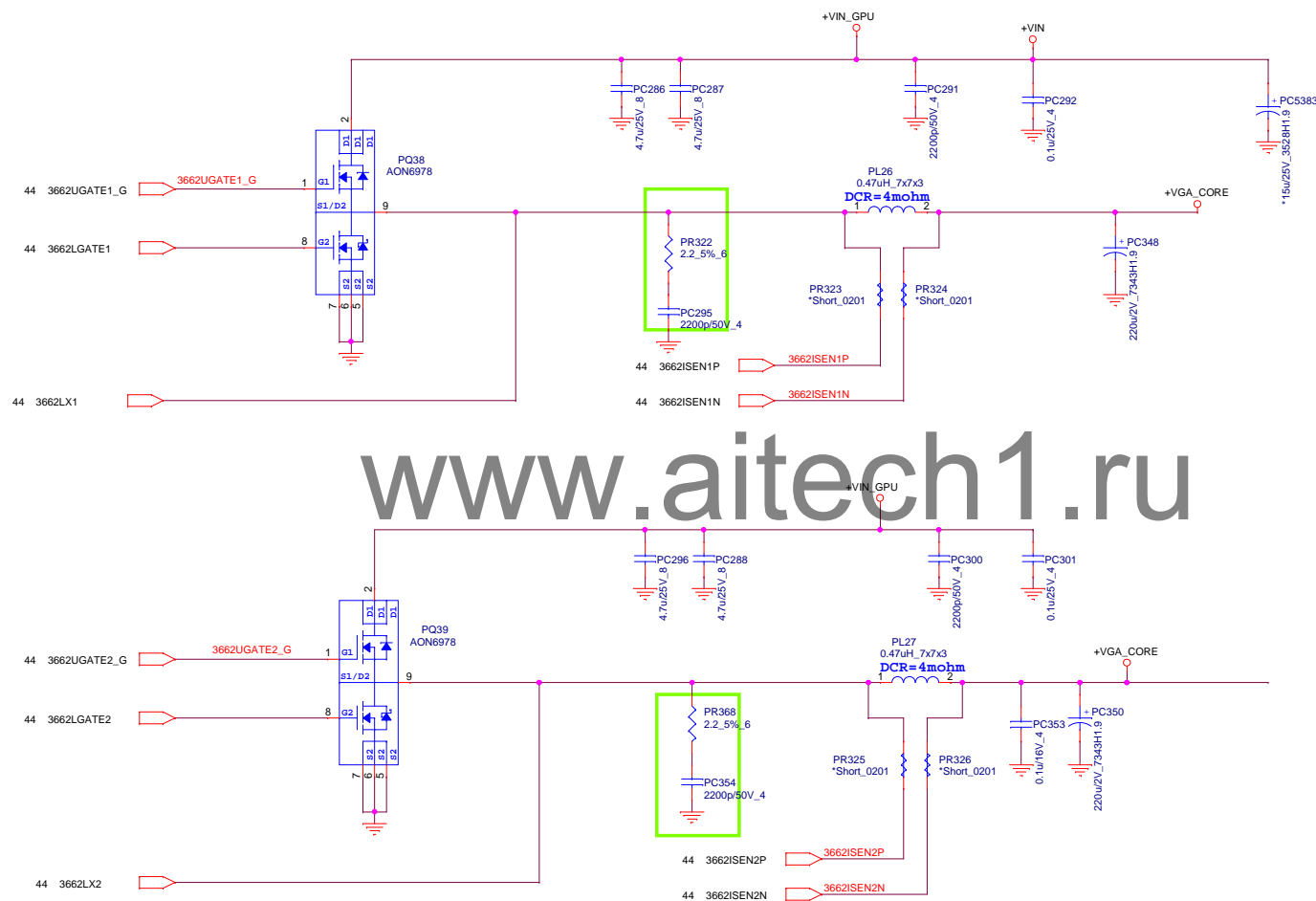




	1 Phase setting	
R1		
R2		
R3		

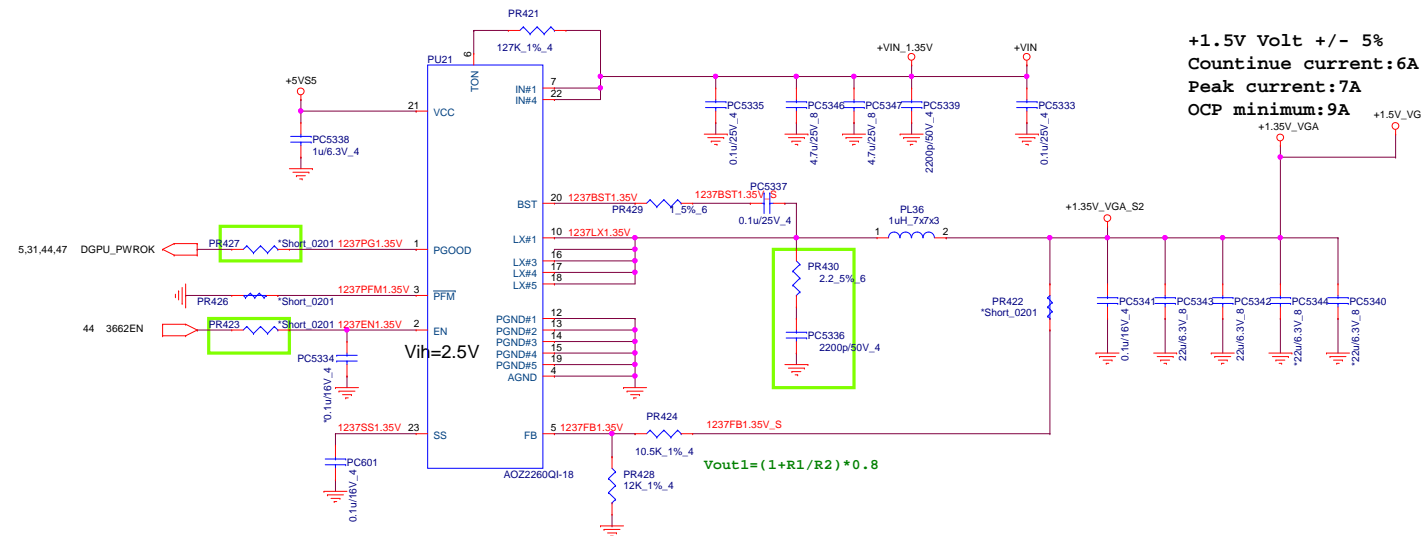
	1 Phase setting	
R4		

	<b>PROJECT : G74(P15-BPA)</b> Quanta Computer Inc.		
	Size Custom	Document Number <b>VGACORE2</b>	Rev 1A
Date: Monday, January 16, 2017	Sheet	45 of 48	

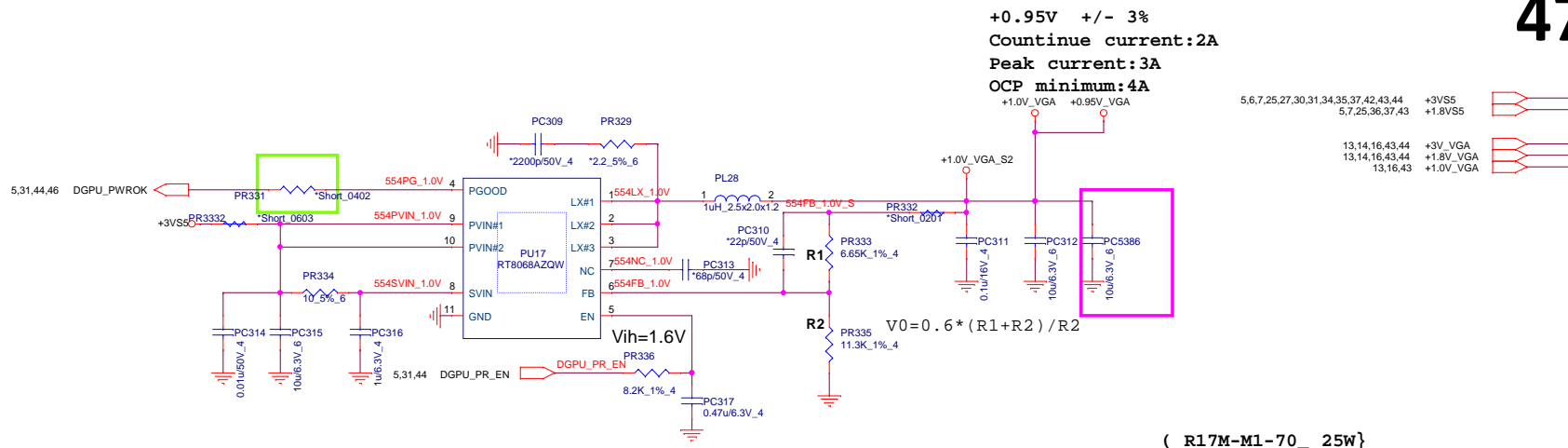


20,30,32,33,34,35,37,38,39,40,41,44,45 +VIN  
22,25,26,28,34,35,36,37,38,40,42,43,44 +5VS5  
16,17,18,19,43 +1.5V\_VGA

Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

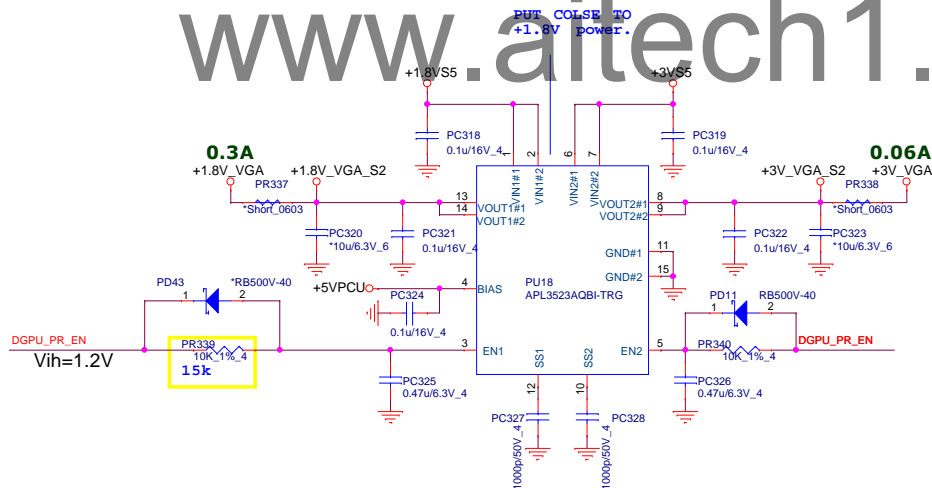


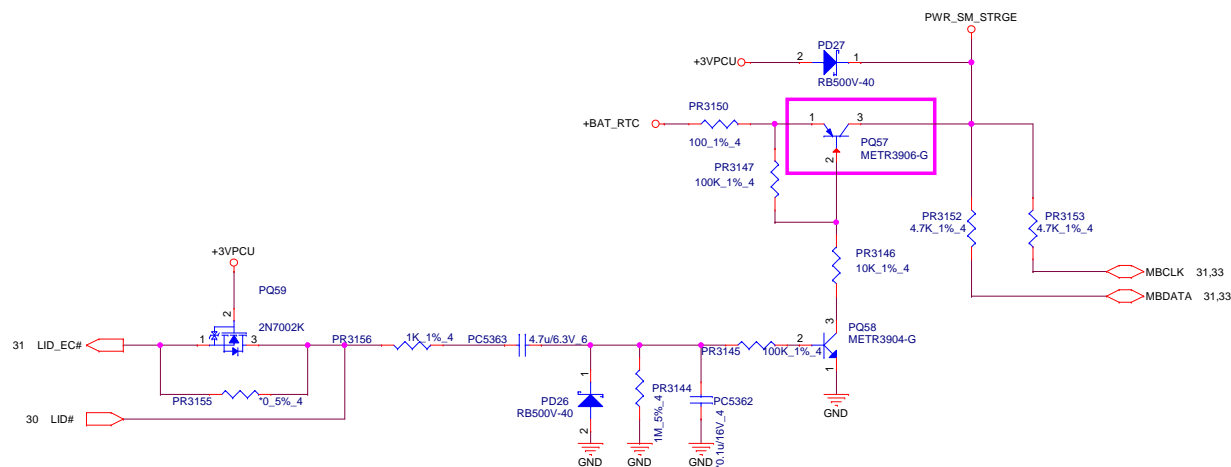
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+3V\_VGA  
 +1.8V\_VGA & +0.95V\_VGA  
 +VGA\_CORE & +1.35\_VGA

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